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# iGp12-400F Signal Processor

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## TECHNICAL USER MANUAL

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## 1 Regulatory Compliance Information

This equipment requires a ground connection provided by the power source. The exposed metal parts of the unit are connected to the power ground to protect against electrical shock. Always use an outlet with properly connected protective ground.

iGp12-400F was designed and tested to operate safely under the following environmental conditions:

- indoor use;
- altitude to 2000 meters;
- temperatures from 5 to 40 °C;
- maximum relative humidity 80% for temperature 31 °C, decreasing linearly to 50% @ 40 °C;
- pollution category II;
- overvoltage category II;
- mains supply variations of  $\pm 10\%$  of nominal.

iGp12-400F contains no user serviceable parts inside. Do not operate with the cover removed. Refer to qualified personnel for service.

**NOTE:** *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**NOTE:** *This Class A digital apparatus complies with Canadian ICES-003. Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.*

## 2 Introduction

### 2.1 Delivery Checklist

1. iGp12-400F chassis;
2. AC power cord;
3. 16-pin ribbon cable;
4. 0.91 m SMA-to-SMA cable;
5. Compact disk with software and documentation;
6. User manual;
7. CE declaration of conformity.

### 2.2 System Overview

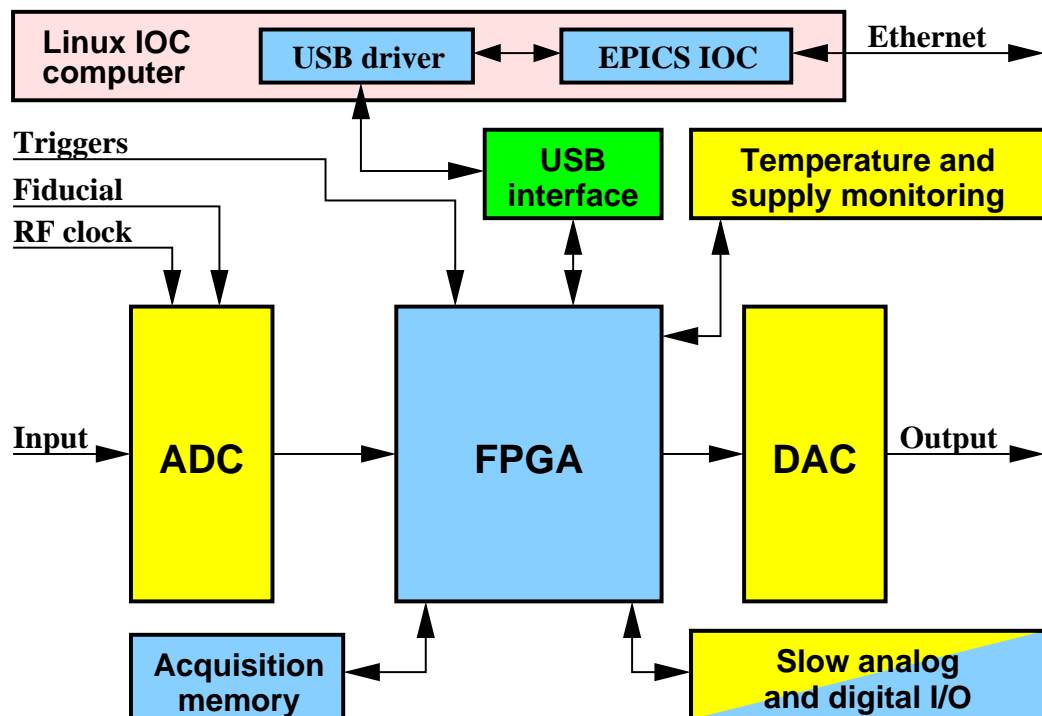


Figure 1: iGp12-400F block diagram

iGp12-400F signal processor is designed for the bunch-by-bunch feedback and diagnostics in lepton storage rings. Functionally iGp12-400F implements a baseband bunch-by-bunch processing channel configured for 400 bunches. Each bunch is processed in a 32-tap finite impulse response (FIR) filter before being sent to the one-turn delay and, from there, to the high-speed digital-to-analog converter (DAC).

A block diagram of the iGp12-400F system is shown in Figure 1. The main signal processing chain consists of a high-speed 12-bit analog-to-digital converter (ADC), a field programmable gate array (FPGA), and a high-speed 12-bit DAC, all driven by the radio frequency (RF) clock. In addition to performing real-time control computations, the FPGA interfaces to a number of on-board devices, such as high-speed data acquisition memory (static random access memory (SRAM)), low-speed analog and digital input/output (I/O), as well as temperature and supply voltage monitors. In turn, the FPGA uses an internal universal serial bus (USB) connection to communicate to an embedded input-output controller (IOC) computer housed in the same chassis. The IOC runs the Linux operating system and is connected to the overall control system via the Ethernet.

### 2.3 Front Panel Features

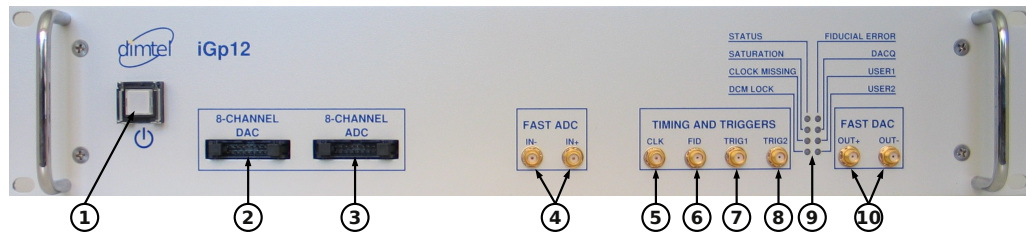


Figure 2: Front panel features

#### 1) Power switch

This momentary-on lighted switch turns iGp12-400F on and off. From the off condition, the unit will take 25–30 seconds to fully boot. Shut-down time after power switch actuation is 3–5 seconds.

#### 2) Low-speed DAC

This 16-pin connector provides 8 general-purpose analog outputs. 14-bit DAC settings are adjustable via experimental physics and industrial control system (EPICS).

#### 3) Low-speed ADC

This 16-pin input connector is provided for measuring up to 8 external analog channels with 12-bit resolution.

#### 4) Fast ADC

Two SMA connectors accept the differential inputs for the high-speed ADC. When a single input is used the full-scale (FS) swing is 780 mV peak-to-peak. Differential mode swing is 390 mV peak-to-peak.

#### 5) RF Clock

This input accepts the high stability bunch crossing clock signal (RF clock). Nominal input level is -3 dBm. The signal is internally AC coupled.

#### 6) Fiducial

This input receives the revolution clock (fiducial). Input threshold is adjustable for a number of standard and custom logic formats. Fiducial is triggered by the falling edge. The signal must be stable within one RF period for reliable operation.



### 7) **Trigger 1**

First of two selectable trigger inputs. Transition threshold is adjustable from EPICS.

### 8) **Trigger 2**

Second trigger input.

### 9) **LEDs**

Eight front-panel LEDs provide indications of system activity and operating status.

#### **STATUS**

FPGA Local bus activity is indicated in green.

#### **SATURATION**

FIR filter operation status. Green indicates normal operation, red — output saturation.

#### **CLOCK MISSING**

Red indication when the input RF clock is not detected.

#### **DCM LOCK**

Lock status of the signal processing digital clock manager (DCM). Green — locked, red — unlocked.

#### **FIDUCIAL ERROR**

Red indication if the fiducial is missing, at the wrong frequency, or jittering.

#### **DACQ**

Data acquisition in progress is indicated by a green LED.

#### **USER1**

External trigger arming indicated in green.

#### **USER2**

Additional status of the signal processing DCM.

### 10) **Fast DAC**

These two differential outputs are generated by the high-speed DAC. For proper operation both outputs must be terminated into 50  $\Omega$ . Output swing is 800 mV peak-to-peak.

### 2.4 Rear Panel Features

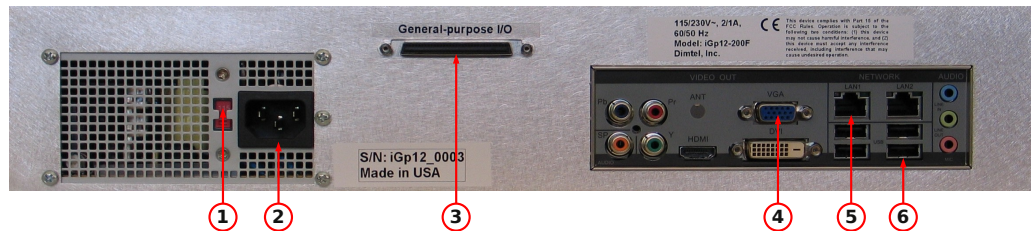


Figure 3: Rear panel features

#### 1) Voltage selection switch

Slide switch for selecting appropriate mains voltage: 115 or 230 V.

#### 2) Power entry socket

IEC-320 power input socket. Always use an outlet with properly connected protective ground.

#### 3) GPIO

This 68-pin connector provides 32 low-voltage transistor-transistor logic (LVTTL) signals for front/back-end interface or future expansion.

#### 4) Monitor output

Connect a monitor for the initial setup of the iGp12-400F.

#### 5) Network

This RJ-45 connector is used to connect the iGp12-400F to the control network. All control and data acquisition communications with the unit are performed via this network connection.

#### 6) USB port

Connect USB keyboard for the initial setup of the iGp12-400F.

## 2.5 Cooling Fan Filter Maintenance

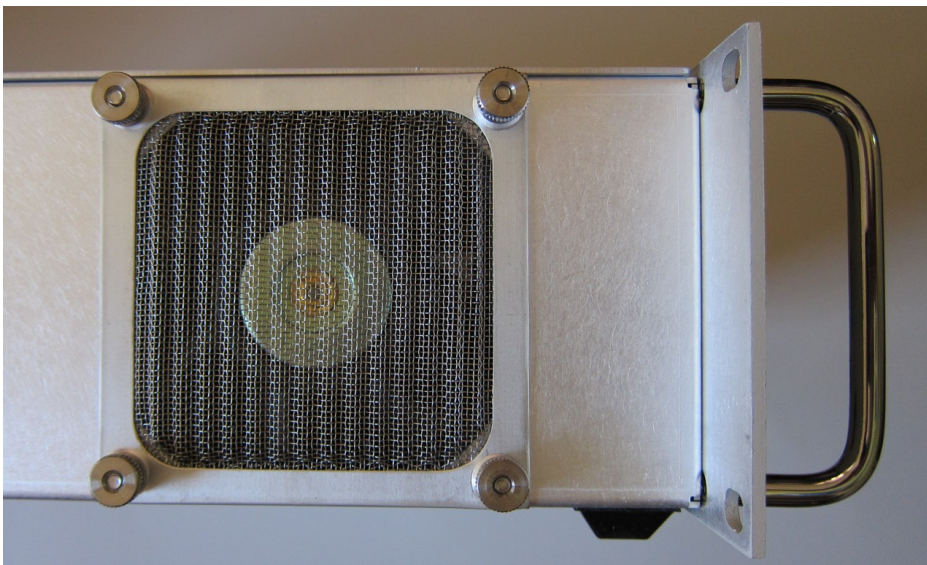


Figure 4: Fan filter mounted using four thumb nuts

Cooling fan is located on the left side of the iGp12-400F. A stainless-steel mesh filter is mounted externally with four thumb nuts.

**WARNING: Fan filter protects the system from contamination. Operating the unit without the filter can lead to overheating as well as to premature failure of the cooling fans.**

**WARNING: Before performing any work on the fan filter, power down the system and unplug the AC power cord. Fan blades are exposed when the filter is removed.**

The filter should be periodically serviced to maintain adequate air flow. Vacuuming, washing or replacement are the acceptable maintenance options. Replacement filter is manufactured by Qualtek Electronics Corporation, part number 06325-M.

In order to remove the filter, undo the four thumb nuts. If filter servicing involves washing, make sure the filter is completely dry before reinstallation. To reinstall, orient the filter so that the mesh corrugations are vertical and slide it onto the mounting studs. Reinstall and hand tighten the thumb screws.

## 2.6 Getting Started

In this section we will present a quick step-by-step guide to get your new feedback processor running in a minimal configuration.

**WARNING:** Before connecting power to the unit make sure the voltage selection switch (Fig. 3, item 1) is in the correct position (115 or 230 V).

1. Configure voltage selection switch (Fig. 3, item 1). Mains supply requirements for the iGp12-400F are listed in Table 10;
2. Connect RF clock at  $-3$  dBm nominal level (Fig. 2, item 5);
3. Connect single-ended high-speed ADC input signal to **Ain+** (Fig. 2, item 4). The FS swing of this signal should be 780 mV peak-to-peak;
4. Connect a  $50\ \Omega$  terminator to **Ain-** (Fig. 2, item 4);
5. Connect high-speed DAC output(s) (Fig. 2, item 10) to the appropriate back-end unit;
6. If single-ended output configuration is used, connect a  $50\ \Omega$  terminator to the unused high-speed DAC output;
7. Connect a USB keyboard (Fig. 3, item 4);
8. Connect a video monitor (Fig. 3, item 5);
9. Push the power button (Fig 2, item 1) to turn on the system;
10. Perform the IOC setup (see Chapter 3);
11. Push the power button (Fig 2, item 1) to turn the system off;
12. Disconnect the keyboard and the video monitor;
13. Connect the Ethernet (10/100/1000BASE-T);

At this point your system is ready for internal testing and use in beam diagnostics and feedback. To extend the configuration beyond the minimum described above one can also connect the external fiducial and trigger signals.

### 3 IOC Setup

Setup program is included in the IOC for configuring the important features of the iGp12-400F. The program can be executed locally or remotely. For local execution one must first connect a keyboard (Fig. 3, item 4) and a video monitor (Fig. 3, item 5) to the system. For remote setup, use **ssh** after system bootup to establish connection. In both setup methods the user must login as **root** (initial password is supplied with the system). If the newly received iGp12-400F must be configured remotely (when, for example, a keyboard or a monitor is not available), such configuration can be performed using a dedicated network. Set up a network consisting of the iGp12-400F, a network hub or a switch, and a remote computer. The iGp12-400F is delivered with the following network configuration:

**IP address** 192.168.1.41  
**Netmask** 255.255.255.0  
**Gateway** 192.168.1.254

Configure the remote computer as follows:

**IP address** 192.168.1.254  
**Netmask** 255.255.255.0  
**Gateway** 192.168.1.41

Once the dedicated network is configured, remote connection to the iGp12-400F can be established by command **ssh root@192.168.1.41**. After logging in locally or remotely, start the setup program as follows:

```
[root@IOC ~]# setup
```

Setup program presents a series of text-mode window dialogs to collect the necessary information for configuring the iGp12-400F. The following settings are configured in this process: timezone, date, time, network, root password, and EPICS device name.

Setup dialogs are illustrated in Figure 5. Here we provide a step-by-step guide through the setup process.

#### a) Welcome panel

This panel provides a summary of settings handled by the setup program.

## IOC Setup

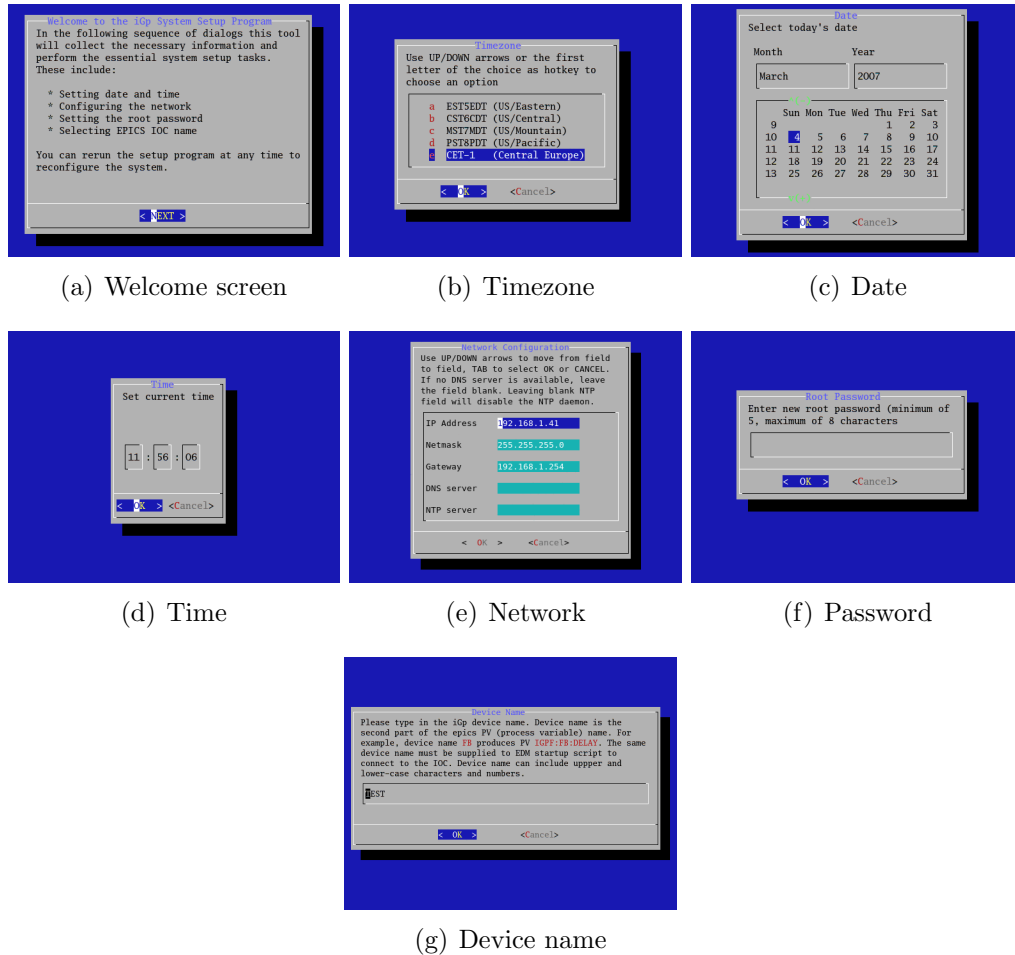


Figure 5: Setup screens

### b) Timezone

In this panel, select the appropriate timezone.

### c) Date

Set the correct date using the calendar.

### d) Time

Set the correct time. The initial setting is taken from the current IOC time. If you know the current IOC time to be correct press OK quickly to retain the setting as closely as possible.

### e) Network

Configure the IOC IP address, network mask and the default gateway as provided by your network administrator. The DNS and NTP server addresses are optional.

**NOTE:** *Only set the DNS address if the server connection is fast and reliable. Delays in DNS server access can negatively impact the operation of the IOC. Typically DNS address is left blank.*

**f) Root password**

Type in the new root password. The password must 5 to 8 characters in length. Please use the standard rules for selecting a strong password (Not based on a dictionary word, a mix of upper and lower-case characters and numbers).

**g) Device name**

This device name is the second part of the EPICS process variable (PV). All PV names start with `IGPF:X:`, where `X` is the device name. As delivered the iGp12-400F defaults to device name `TEST` producing PVs of the form `IGPF:TEST:DELAY`. If multiple iGp12-400F units are to be deployed they must be assigned differing device names. For example, one could use device names `X`, `Y`, `Z` for horizontal, vertical, and longitudinal feedback channels.

**NOTE:** *If the setup program is executed remotely and the network address is changed, the `ssh` connection will hang at the end of the process. To connect to the IOC, close the existing `ssh` session and start the new connection at the newly assigned IOC IP address.*

## 4 Utilities and Selftest

### 4.1 Utilities

The IOC includes several utilities designed to communicate to the iGp12-400F directly, without using the EPICS softIOC software. These utilities allow the user to access individual FPGA registers and memory locations. For register descriptions and address map see Sec. 9. All of the utilities below will accept addresses and data in decimal, hex, if preceded by `0x`, and octal, if the value starts from 0. For example, value 12 can be specified as 12, `0xc`, or `014`. In order for these utilities to gain access to the FPGA interface the IOC process must be terminated. To terminate the IOC execute:

## 4.2 Selftest

---

```
[root@IOC ~]# pkill -9 st.cmd
```

Here is a short description of the available commands:

**usbr <addr>**

Read a single register or memory location.

**usbw <addr> <val>**

Write a single location.

**usbrblk <addr> <len>**

Read a block of memory. The data is sent to **stdout** and can be redirected into a file.

**usbwblk <addr> <len>**

Write a block of memory. This utility expects the data from **stdin**.

**memtest <addr> <len> <cnt>**

Test the register or memory block specified by the **addr,len** combination. The utility generates a block of random numbers and writes it to the FPGA. Then the data is read back and compared to the original values. Argument **cnt** specifies the number of test cycles to perform.

## 4.2 Selftest

Another important utility included in the IOC is **selftest**. This program performs testing of the main signal path, memories, and peripherals. In order to perform the testing system hardware must be configured as follows:

- Connect the 16-pin ribbon cable between the 8-channel DAC (Fig. 2, item 2) and the 8-channel ADC (Fig. 2, item 3);
- Connect 499.66 MHz clock to the RF clock input (Fig. 2, item 5);
- Terminate Ain- fast ADC input (Fig. 2, item 4);
- Terminate Aout- fast DAC output (Fig. 2, item 10);
- Connect a 6 dB attenuator to Aout+ fast DAC output;
- Connect the output of the attenuator to Ain+ fast ADC input using the supplied SMA-SMA cable;
- Make sure no cable is connected to the general-purpose digital I/O port (Fig. 3, item 3);
- Make sure fiducial input is not driven (Fig. 2, item 6);



Once the hardware is configured the test procedure can be initiated by typing `selftest` at the IOC command prompt (establish local or remote connection to the IOC as described in Sec. 3). Example output of the test is shown below:

```

1 Terminating the IOC
2
3 System information:
4   Function:          feedback
5   Harmonic number: 120
6   Demultiplexing:   UES
7   Revision:         1.00
8   Serial number:    IGP12-0001
9
10          STARTING THE AUTOMATED TEST SEQUENCE
11
12 Testing internal blockRAM: [OK]
13 Testing external SRAM: USB: [OK]
14 Testing external SRAM: DACQ: [OK]
15 Testing general-purpose digital inputs/outputs: [OK]
16 Verifying RF clock presence and DCM lock: [OK]
17
18 Testing low-speed DAC/ADC system
19 Ch(ADC) ADC(mV) DAC(mV) Off(mV) DAC(mV) ADC(mV)
20 0      -2048   -2068     -1    2069    2047
21 1      -2048   -2077     10    2056    2046
22 2      -2048   -2074     9     2055    2046
23 3      -2048   -2070     -2    2072    2047
24 4      -2048   -2081     6     2068    2047
25 5      -2048   -2064     -3    2068    2047
26 6      -2048   -2072     6     2061    2047
27 7      -2048   -2067     4     2062    2047
28
29 Testing high-speed DAC offset channel
30 Offset DAC(cnt) Fast ADC(cnt)
31 -8192          -191.0
32 252            -0.4
33 8191           179.0
34
35 Testing high-speed DAC output
36 HS DAC(cnt)    HS ADC(cnt)
37 -2048          -827.3
38 0              -0.1
39 2047           825.9
40

```

## 4.2 Selftest

---

41	Environmental measurements	
42	Bulk supply voltage (12V):	12.07
43	Vcc supply voltage (3.3V):	3.29
44	FPGA core supply voltage (1.0V):	0.99
45	Analog 5V supply voltage (5.0V):	4.97
46	Analog 3.3V supply voltage (3.3V):	3.29
47	iGp board temperature (deg C):	27.4
48	FPGA temperature rise (deg C):	3.7
49	ADC clock delay temperature rise (deg C):	4.7
50	DAC clock delay temperature rise (deg C):	7.7

### Line 1

The utility terminates the IOC process to gain access to the FPGA interface.

### Lines 3–8

Contents of the FPGA config register are parsed and printed out.

### Line 12

Test of the data acquisition blockRAM.

### Line 13

SRAM is tested via the local bus.

### Line 14

SRAM is tested with the ADC data test pattern generator.

### Line 15

General-purpose digital I/O is tested.

### Line 16

Presence of the RF clock is verified as well as the lock status of the DCMs.

### Lines 18–27

A test of the low-speed DAC and ADC system. This test uses 8 channels of the DAC to drive different voltages and measures the voltages using the ADC. The test measures several parameters for each channel. Test code finds the minimum DAC setting that does not saturate the ADC. ADC reading (column 2) and the dead-reckoned DAC output (column 3) are printed out in millivolts. Next the DAC is set to 0 and the ADC reading (offset, column 4) is taken. Finally, the code finds the maximum DAC setting that does not saturate the ADC.

**Lines 29–33**

This portion of the test uses a dedicated offset DAC to adjust the output offset of the high-speed DAC. The code extracts the reading from the high-speed ADC at the positive and negative extremes of the offset DAC. Next the code finds the offset DAC setting that minimizes the high-speed ADC measurement. This setting should be very close to the factory determined value used in EPICS to null the high-speed DAC output.

**Lines 35–39**

This fragment verifies the response via the high-speed DAC. To do so it finds the ADC response at DAC settings of  $-2048$  and  $2047$ , as well as the DAC setting that produces 0 counts from the ADC.

**Lines 39–47**

Environmental monitor readings are taken and displayed.

The output of `selftest` utility can be redirected to a file and compared to the factory measurement provided in `/root/factory.selftest`.

After testing restart the IOC process by typing:

```
[root@IOC ~]# iGp_start -nofw
```

**NOTE:** *Command-line switch `-nofw` avoids reloading FPGA gateway*

## 5 User Interface

User interface functionality for the iGp12-400F is implemented using extensible display manager (EDM). Software installation CD is designed for seamless installation on a client computer running one of the 32 bit versions of Linux operating system listed in Table 1.

**Table 1: Supported Linux distributions**

Distribution	Versions
Red Hat Enterprise Linux	5
Scientific Linux	5.5
CentOS	5.5
Fedora	11–13

### 5.1 Installation

- Log into the client computer.
- Insert the installation CD into the CD-ROM drive.
- Mount the CD by accepting the "Open in New Window" option or by right clicking on the CD icon and selecting "Mount".
- Open a terminal window.
- Issue the following installation command:  
`sudo sh <CD mount point>/install.sh`. Typically CD mount point will be `/media/iGp`. *Note: to install the software one must have superuser privileges, obtained either via `sudo` or `su`.*
- When prompted, enter the user name to install under. If the specified user does not exist it will be created. Default user name is *iGp*.
- When prompted, enter the installation directory. Default directory is *iGp*.
- If the specified user did not exist, the program will prompt for password.
- Wait for the installation process to complete.

The resultant installation can support multiple IOCs with distinct device names. Refer to Section 3 for a definition of the device name. Each IOC must be added to the configuration. To do so, log in under the username, specified during software installation (EPICS user). Open a terminal and type:

```
[iGp@host ~]$ IOC_add <IP address> <device name>
```

**WARNING: IOC and the client computer must be able to communicate at this point, otherwise IOC\_add will fail.**

After adding one or more new IOCs to the configuration the user must log out and log back in for the changes to take effect.

### 5.2 Starting the EDM

Once the software has been installed and the IOCs added via `IOC_add` you are ready to start the EDM. iGp12-400F display panels are opened by the following command:

```
[iGp@host ~]$ iGp_display [-r 8|12] [device name]
```

Note that the device name is optional. If the argument is omitted the command defaults to device name **TEST**. Optional argument **-r** can be used to select 8 or 12-bit versions of the iGp displays (iGp or iGp12 respectively). Without the command-line switch, **iGp\_display** determines the appropriate version by examining the FPGA revision reported by the system.

### 5.3 Bunch Pattern Specification

Several fields in iGp interface (feedback, drive, bunch cleaning, and spectral averaging patterns) use common bunch pattern specification format. The syntactic structure of this format allows three types of elements: single bunch number, range, range with a step. Individual elements should be separated by spaces. Single bunch number element is an integer in the range from 1 to 400. A range is specified as **start:stop**. Range can wrap around, that is if **stop** is smaller than **start**, the range covers **1:stop start:400**. To specify a range with a step use **start:step:stop** construct. For example, drive pattern of **[2:2:400 1:10 13]** includes all even bunches, range from 1 to 10, and bunch 13. If the first element of the pattern is **!**, the pattern is inverted, that is only listed elements are excluded. A pattern of **[!3 4]** includes all bunches except 3 and 4.

Each of the main three pattern fields (feedback, drive, and spectral averaging) generates an enable mask vector, described in more detail in Sec. 5.4. In order to disable pattern strings and to use the masks directly, set the first character of the pattern string to **-** (hyphen-minus).

### 5.4 Bunch Enable Masks

iGp user interface provides two ways of specifying bunches for feedback, drive, and spectral averaging: bunch pattern specification and the mask vector. Bunch pattern specification language described above provides a powerful compact way to define many common patterns. In certain cases, however, it is desirable to have direct access to bunch-by-bunch enable mask vector.

There are three mask vectors in the iGp: **FB:MASK**, **DRIVE:MASK**, and **ACQ:MASK** (each PV starts from the same prefix, e.g. **IGPF:TEST:**). The number of elements in each vector is defined by the harmonic number of the ring. Each vector element defines the enable bit for a particular bunch. Set element value to 1 to enable the action and to 0 to disable.

## 5.5 Data Acquisition Capabilities

iGp12 is configured with three independent data acquisition engines: two multi-bunch and one single-bunch. One multi-bunch unit uses on-board SRAM memory with 12M samples capacity. The second multi-bunch unit drives a much smaller blockRAM memory within the FPGA (276k samples). Both of these acquisition engines support pre- and post-trigger acquisition, grow/damps, internal and external triggers. In standard operation, SRAM is typically used with the external trigger in pre-trigger acquisition mode to capture beam abort transients. Real-time updates on beam stability, RMS, and spectra are normally provided by the BRAM acquisition engine. SRAM acquisitions have a maximum update rate of  $2 \text{ s}^{-1}$ , while BRAM supports  $5 \text{ s}^{-1}$ .

The third data acquisition engine acquires 96k samples for a single bunch. This unit supports post-trigger acquisition with internal or external trigger sources. It also captures the excitation output parameters at the start of the acquisition. IOC analysis routines can use that information to compute a beam transfer function. Single-bunch acquisition engine updates once a second.

It is possible, but not advisable to run both multi-bunch acquisition engines from internal trigger at the same time. They will compete for bus bandwidth and CPU processing time, reducing the performance.

## 5.6 Display Panels

### 5.6.1 Main Panel

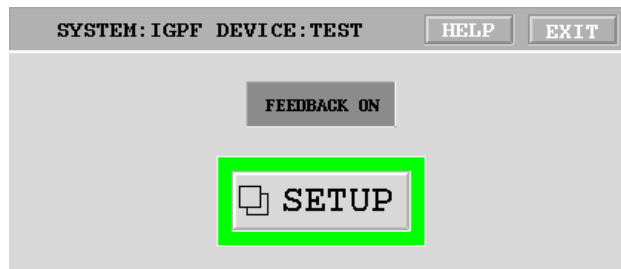


Figure 6: Main (top-level) panel

Running `iGp_display` brings up the top-level panel shown in Figure 6.

All of the display panels include two buttons on the top: *HELP* and *EXIT*. *EXIT* button will always close the current window. In addition, *EXIT* button on the top-level panel will close the EDM session.

Top-level panel consists of three elements: *FEEDBACK ON/OFF* control, *SETUP* button and the status border around this button. The *FEEDBACK ON/OFF* control enables or disables the FIR filter output to the DAC. The status border indicates system operational status summary. **Green** indicates no errors, **yellow** - warning (saturation), **red** - error. The *SETUP* button opens the control panel shown in Fig. 7.

### 5.6.2 Control Panel

The screenshot shows a control panel window titled "ID=IGPF:TEST". It features a "FEEDBACK SETTINGS" section with four adjustable parameters: "COEFFICIENT SET" (Set 0), "SHIFT GAIN" (1), "DOWNSAMPLING" (1), and "SAT. THRESHOLD" (0.00 %). To the right of these settings is a grid of buttons for various system functions: "Coefficients", "Timing", "SRAM control", "BRAM control", "SB control", "Environment", "Devices", "Drive", "SRAM waveforms", "BRAM waveforms", "SB waveforms", "Config S/R", and "Front/back-end". Below the settings is a "STATUS" section with six green indicator boxes: "Clock missing", "PLL unlocked", "DCM unlocked", "ADC overrange", "Output saturated", and "Fiducial error", each with a "0" below it. At the bottom, there is an "Interval (sec)" field showing "85" and a "COUNT" button.

Figure 7: Control panel

This window integrates most important controls for the iGp12-400F.

#### COEFFICIENT SET

Feedback coefficient set selector.

#### SHIFT GAIN

Output gain adjustment. This adjustment is performed by shifting FIR output word left by a specified number of positions. Thus, increase by one in this setting doubles the feedback gain.

#### DOWNSAMPLING

Processing channel downsampling factor.

#### SAT. THRESHOLD

iGp12-400F is equipped with an integrating saturation counter. The counter is compared with a threshold duty cycle, expressed here in



percent. A setting of 50% indicates that the output was saturated half the time. On every poll cycle (once a second) the threshold comparison result is read out and the counter is reset to 0. Setting this field to a value of 0 produces single saturation event detector within a polling period.

**Coefficients**

Opens FIR coefficients control panel.

**Devices**

Opens the control panel for the integrated devices.

**Timing**

Opens timing control panel.

**Drive**

Opens the drive control panel.

**SRAM Control**

Opens the SRAM acquisition engine control panel.

**SRAM Waveforms**

Opens the waveform display panel for the SRAM acquisition engine.

**BRAM Control**

Opens the BRAM acquisition engine control panel.

**BRAM Waveforms**

Opens the waveform display panel for the BRAM acquisition engine.

**SB Control**

Opens the single-bunch acquisition control panel.

**SB waveforms**

Opens the waveform processing and display panel for the single-bunch acquisition engine.

**Environment**

Opens the environmental monitoring panel.

**Config S/R**

Configuration save/restore panel.

**FB ID**

Device ID string for the iGp/iGp12 unit controlling the 3-channel combination front/back-end unit (FBE-LT).

**Front/back-end**

Open general-purpose interface panel, controlling FBE-LT. Value of the device ID string, specified under **FB ID** is used select the appropriate IOC. In full ring installations, with longitudinal, horizontal, and vertical channels, FBE-LT is normally controlled by the longitudinal baseband processor. Using **FB ID** the user can configure all three systems to point to the one active FBE-LT control panel of three possible.

**Clock missing**

RF clock missing indicator.

**PLL unlocked**

Signal processing phase-locked loop (PLL) lock indicator.

**DCM unlocked**

Local bus DCM lock indicator.

**ADC overrange**

ADC input signal exceeds the full-scale range of the device.

**FIR saturation**

FIR filter output saturation duty cycle exceeds the threshold level.

**Fiducial error**

Indicates missing or jittering fiducial.

**Interval**

Number of polling cycles (seconds) since the last error counter reset.

**COUNT**

Reset error and interval counters.

## 5.6.3 Coefficients Panel

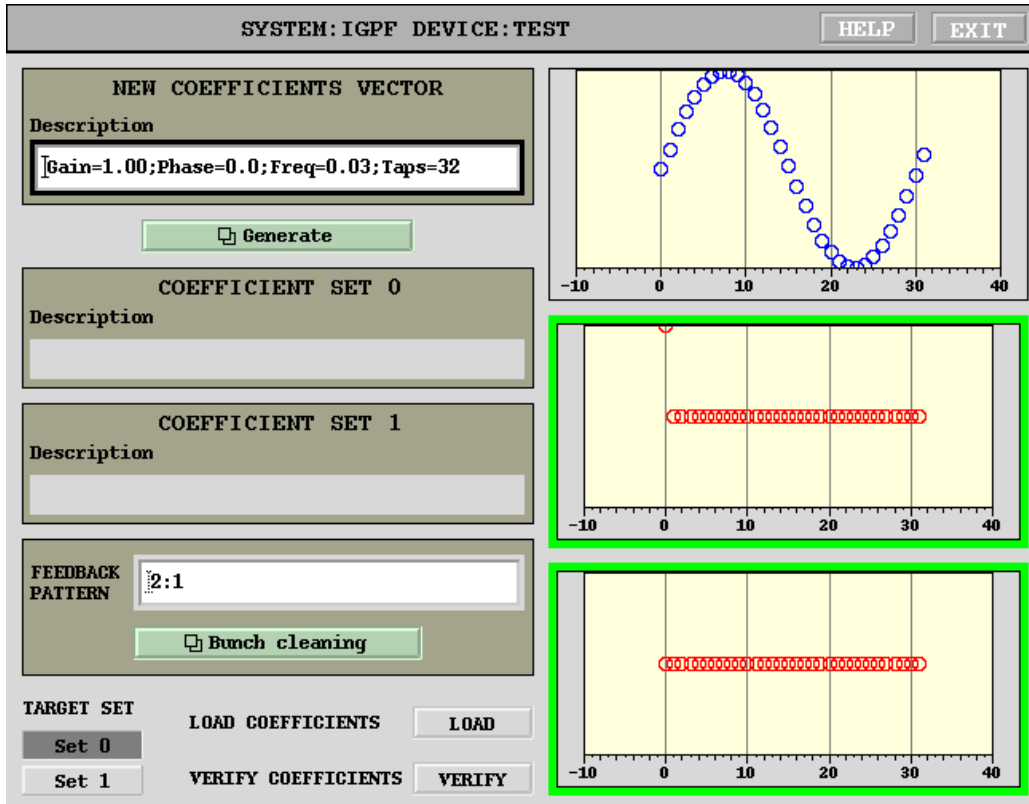


Figure 8: Coefficients panel

Coefficients control panel allows the user to manipulate the loaded coefficients sets and verify that the hardware is in sync with the panel display. The panel is split into three functional groups: new coefficients vector, coefficient set 0, and coefficient set 1. The first group shows the coefficient vector and its description generated using coefficient generator panel (Fig. 9). This vector can be loaded into hardware coefficient sets 0 or 1. Colored borders around the hardware coefficient displays indicate the results of coefficient verification. Green shows that the readback is in agreement with the EPICS values.

**Generate**

Opens the coefficient generator panel.

### **FEEDBACK PATTERN**

This field enables the feedback output for the specified bunch pattern. Bunch specification format is described in Section 5.3.

### **Bunch cleaning**

This button opens the bunch cleaning panel.

### **TARGET SET**

Selects which set the new coefficient vector is to be loaded.

### **LOAD COEFFICIENTS**

Loads the new vector to the hardware coefficient set specified by *TARGET SET*.

### **VERIFY**

Verifies coefficient sets 0 and 1 against hardware values.

### 5.6.4 Coefficient Generator Panel

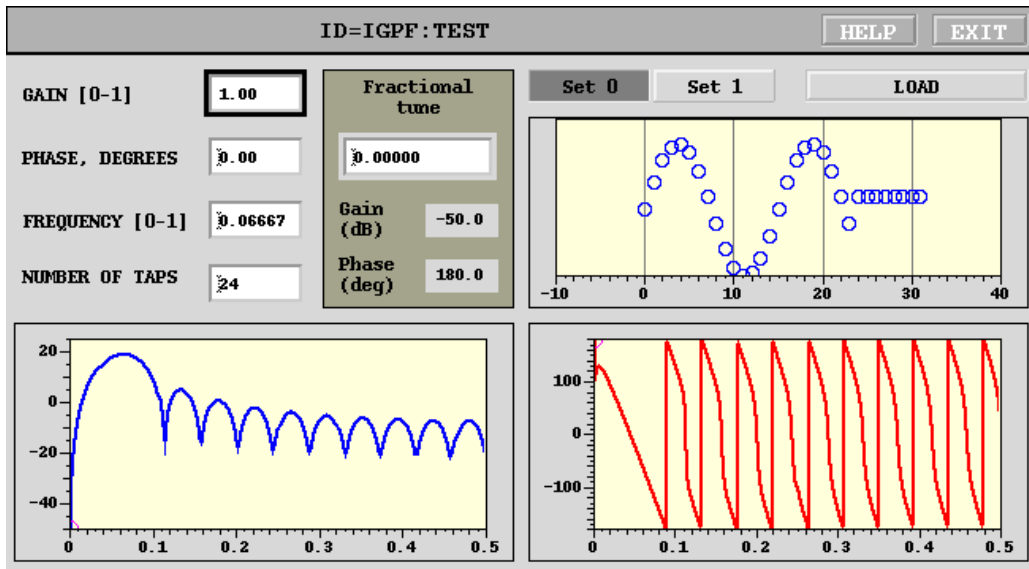


Figure 9: Coefficient generator panel

Coefficient generator panel shown in Figure 9 allows the user to generate feedback processing controllers and explore different delay/gain/bandwidth tradeoffs. This tool generates a coefficient set based on sampling a sine wave. Transfer function of the filter is computed and displayed together with an adjustable marker.

#### **GAIN**

Filter gain in the range from 0 to 1.

#### **PHASE**

Filter phase in degrees.

#### **FREQUENCY**

Center frequency in fractional tune units. Multiply this by the revolution frequency to get the physical center frequency.

#### **NUMBER OF TAPS**

Number of filter taps.

**Fractional tune**

Marker frequency.

**Gain (dB)**

Gain at the marker frequency in dB.

**Phase (deg)**

Phase at the marker frequency in degrees.

Buttons for selecting target coefficient set and to load the coefficients are included on this panel for the operational ease. See 5.6.3 for full description of their functionality.

### 5.6.5 Bunch Cleaning Panel

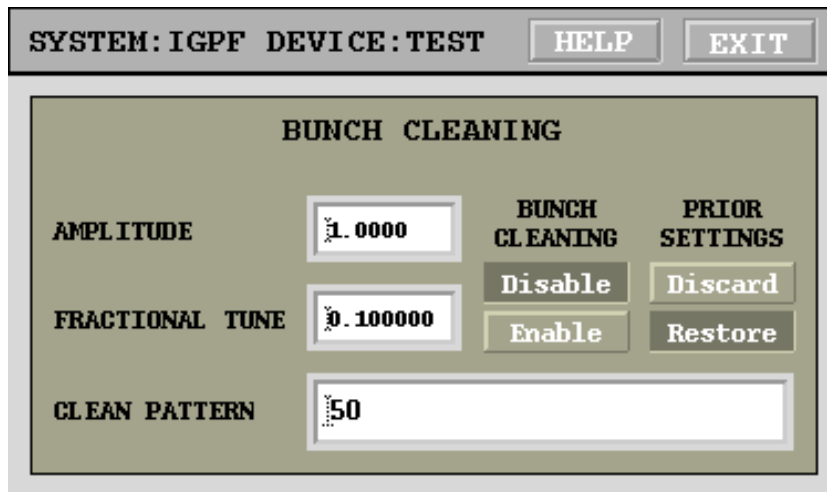


Figure 10: Bunch cleaning panel

Bunch cleaning panel shown in Figure 10 provides a single-point interface to configure both feedback and bunch cleaning controls. When bunch cleaning is enabled, drive pattern is loaded with the cleaning pattern. Simultaneously the feedback pattern is set to the complement of the drive pattern, that is each bunch is either driven (cleaned) or controlled by feedback. Drive amplitude and frequency are set to the values defined in the cleaning panel. Drive signal is set to a sinewave.

#### AMPLITUDE

Cleaning signal amplitude, 0 to 1.

#### FRACTIONAL TUNE

Fractional tune, 0 to 1.

#### CLEAN PATTERN

Bunch pattern to clean - all other bunches are set to feedback.

#### BUNCH CLEANING

Cleaning enable control.

#### PRIOR SETTINGS

When bunch cleaning is enabled, it saves drive panel settings and the

## 5.6 Display Panels

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feedback pattern. If this selector is set to restore, when bunch cleaning is turned off these saved values will be restored.



### 5.6.6 Timing Panel

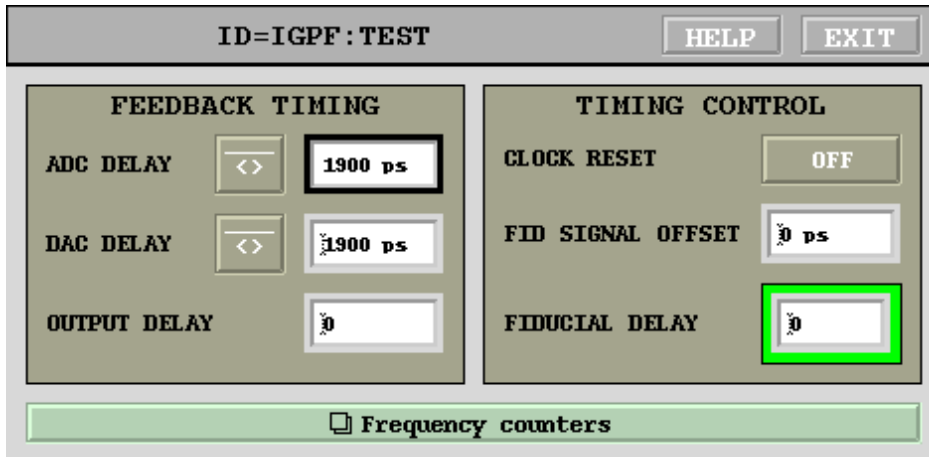


Figure 11: Timing panel

This window provides controls for system timing.

#### ADC delay

High-speed ADC clock delay in picoseconds. This adjustment is independent of the back-end timing (DAC delay) and has a range from 0 to  $T_{\text{rf}} - 1$  ps. Rounding to 10 ps adjustment step size is handled automatically.

#### DAC delay

High-speed DAC clock delay in picoseconds. This adjustment is independent of the front-end timing (ADC delay) and has a range from 0 to  $T_{\text{rf}} - 1$  ps. Rounding to 10 ps adjustment step size is handled automatically.

#### OUTPUT DELAY

High-speed DAC output delay in units of RF periods.

#### CLOCK RESET

Pushbutton for resetting feedback processing and data acquisition PLL. Push this button if *PLL unlocked* indicator is red and the RF clock is present at the iGp12-400F front panel. On rare occasions due to intermittent RF clock loss PLL might need to be reset even though

## 5.6 Display Panels

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lock indicators are green. If PLL misbehavior is suspected, check the frequency counters, described below.

### FID SIGNAL OFFSET

This offset sets the relative timing of the input fiducial signal and the fiducial receiving clock. This setting must be optimized after installation. To do so, connect the RF clock and the fiducial in the final (operational) configuration. Then, adjust the fiducial delay to find the error range. Let us consider, for example, RF frequency of 368 MHz. The RF period is 2700 ps. Within one period there should be a range of delays in which the fiducial is jittering across the RF clock and the fiducial error indicator is red. By moving the delay in steps of 100 ps find the beginning ( $N_1$ ) and the end ( $N_2$ ) of this range. The optimal setting is at  $(N_1 + N_2)/2 \pm 1350$  ps.

### FIDUCIAL DELAY

Input fiducial delay in single bunch steps. Use to place bunch 1 signal in channel 1 of the data acquisition. For example, if bunch 1 signal is seen in acquisition channel 6, increment this field by 5.

#### 5.6.7 Frequency Counter Panel

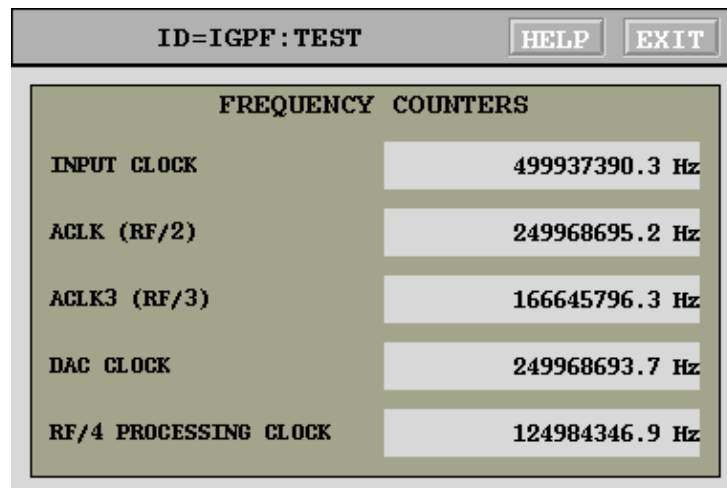


Figure 12: Frequency counter panel

iGp12-400F gateway uses internal local-bus clock to measure the frequencies of various signal processing clocks. Raw input clock as well as some PLL-derived ones are monitored.

**INPUT CLOCK**

This clock should correspond to your RF frequency.

**ACLK (RF/2)**

Signal processing PLL output at  $f_{\text{RF}}/2$ .

**ACLK3 (RF/3)**

PLL clock at  $f_{\text{RF}}/3$ , used for data acquisition.

**DAC CLOCK**

DAC clock signal at  $f_{\text{RF}}/2$ .

**RF/4 PROCESSING CLOCK**

Filtering and control at  $f_{\text{RF}}/4$ .

### 5.6.8 Drive Panel

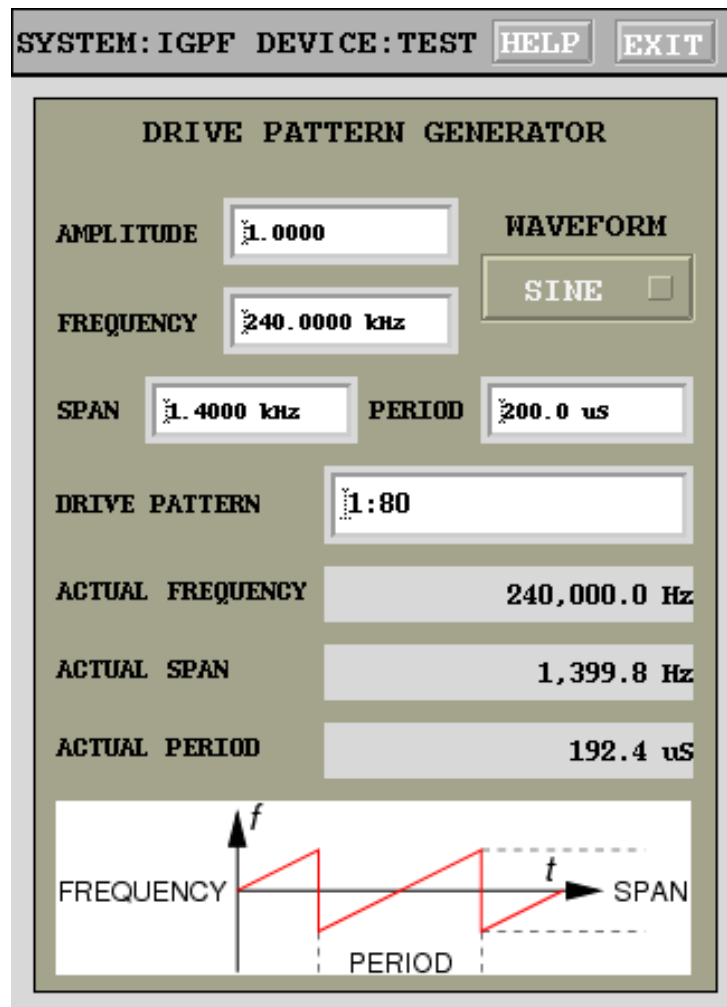


Figure 13: Drive panel

Drive panel shown in Figure 13 provides the means to generate an excitation signal on a bunch-by-bunch basis. The drive output has many applications:

- Back-end timing;
- Kicker gain checking;

- Excitation source for front-end timing;
- Bunch cleaning.

**AMPLITUDE**

Drive amplitude in the range from 0 to 1 (sine or square wave). For DC output mode, the range is  $-1$  to  $1$ .

**FREQUENCY**

Drive frequency in Hz. Drive signal generator has frequency step size of  $f_{\text{rf}}/2^{30}$ .

**WAVEFORM**

Waveform selector allows the user to drive the beam with sine, square, and DC signals.

**SPAN**

In sine- and square-wave modes the drive generator can be frequency modulated (swept) as illustrated on the bottom of the panel. This field sets the sweep span in kHz. Setting span to 0 disables frequency modulation.

**PERIOD**

This field sets the sweep period in microseconds. Setting period to 0 disables frequency modulation.

**DRIVE PATTERN**

Drive pattern string selects bunches to be driven.

**ACTUAL FREQUENCY**

Drive frequencies are quantized with step size  $f_{\text{rf}}/2^{30}$ . This field reads out the actual drive frequency which is the closest possible approximation to the value, specified in *FREQUENCY*.

**ACTUAL SPAN**

Actual frequency span in use.

**ACTUAL PERIOD**

Actual sweep period in use.

### 5.6.9 Data Acquisition Controls

The screenshot shows a control panel titled "ID=IGPF:TEST:SRAM" with "HELP" and "EXIT" buttons. The main section is "DATA ACQUISITION".

- GROW/DAMP ENABLE:** A button labeled "OFF". To its right are "SRAM" and "BRAM" buttons.
- REC. DOWNSAMPLE:** A numeric input field showing "1". To its right is a "RAW DATA" button labeled "OFF".
- ACQUISITION TIME:** A numeric input field showing "15.0 ms".
- HOLD-OFF TIME:** A numeric input field showing "0.0 ms".
- POST-TRIGGER:** A numeric input field showing "0.0 ms", which is highlighted with a green border.
- GROWTH TIME:** A numeric input field showing "9.0 ms", which is highlighted with a green border.
- ACQUISITION LENGTH:** A display showing "93664 turns".
- POST-TRIGGER LENGTH:** A display showing "0 turns".
- ACQ TYPE:** A button labeled "PRE/POST".
- TRIGGER:** A section with buttons for "INT", "EXT", "TRIG1", and "TRIG2". Below these are "Arm" (OFF), "Auto re-arm" (OFF), and a "RESET" button followed by two numeric input fields showing "0" and "0".

A "Waveforms" button is located at the top right of the panel.

Figure 14: Data acquisition control panel

Each data acquisition engine is managed by an individual control panel. Panels are identical, with the only difference being the time units. SRAM panel uses milliseconds, while microseconds are indicated on the BRAM one.

#### GROW/DAMP ENABLE

Enables coefficient set switching during data acquisition. Only one data acquisition engine can control the coefficient set.

#### REC. DOWNSAMPLE

Acquisition channel downsampling factor. This downsampling process is completely decoupled from the processing channel downsampling.

#### RAW DATA

This button dumps the raw data from the last acquisition into a waveform PV (:SRAM:RAW or :BRAM:RAW), so that it can be read out by external interface tools.

**ACQUISITION TIME**

Acquisition time duration. Maximum acquisition length is defined by the RF frequency, downsampling factor, and memory depth (12M samples for SRAM, 276k samples for BRAM).

**HOLD-OFF**

Time duration to keep the coefficient set select inverted before data acquisition. This can be used to delay data acquisition and give slow oscillations time to grow.

**POST-TRIGGER**

Portion of the data acquisition process that takes place after the trigger even. This value can range from 0 (pure pre-trigger acquisition) to the full acquisition time value (pure post-trigger).

**GROW LENGTH**

Time length to hold the coefficient set select inverted during data acquisition, if enabled by the grow/damp selector.

**ACQUISITION LENGTH**

Computed acquisition length is reported in this field in the units of turns. Note that with downsampling, number of turns corresponds to the actual acquired data, not real-time.

**POST-TRIGGER LENGTH**

Computed post-trigger length is reported in this field in the units of turns.

**Waveforms**

Opens the appropriate waveform display panel.

**ACQ TYPE**

This toggle can be used to quickly switch the acquisition to post-trigger mode. If post-trigger mode is enabled, value of the **POST-TRIGGER** field is not used - all data is acquired after the trigger.

**TRIGGER INT/EXT**

Acquisition trigger source, internal or external.

**TRIG1/TRIG2**

Selects external trigger source input.

### **Arm**

External trigger is only valid if the acquisition system is armed. Single-event acquisitions on the external trigger can be performed by pushing this button.

### **Auto re-arm**

This option re-arms the acquisition system after each data readout. This allows for continuous updates of beam data triggered by external signal. Note that the first acquisition on external trigger must be armed manually.

### **Trigger capture**

Two bit readouts in the lower right capture the external trigger input states at the time the last acquisition was triggered. These are FPGA-internal trigger levels — if the falling edge is selected for a particular signal, captured level is inverted relative to the physical input state.



## 5.6.10 Waveforms Panel

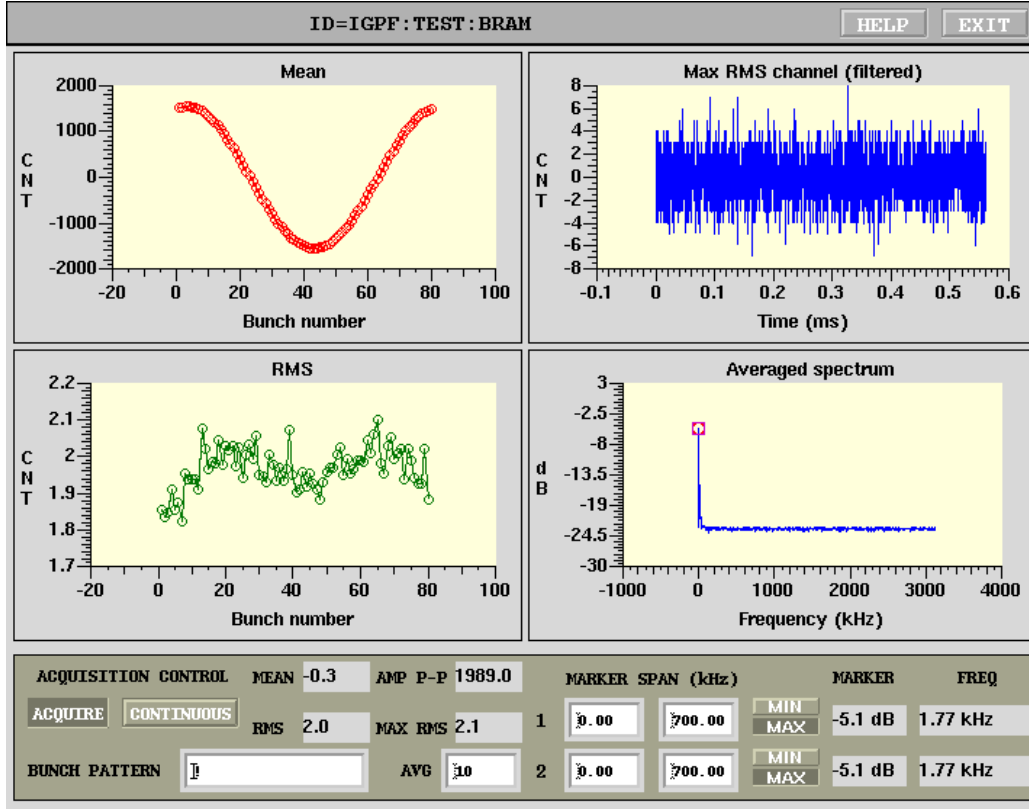


Figure 15: Waveforms panel

A set of IOC subroutines postprocesses the data in the real-time and provides four concise plots displayed in the waveform panel shown in Figure 15. The four plots are: bunch-by-bunch mean and root mean square (RMS) of bunch oscillations, time-domain signal of a bunch with the largest RMS. The last plot is obtained by performing the fast Fourier transform (FFT) on each of the bunches (specified by a selection pattern) and quadratically averaging the resulting spectra. This plot aliases all coupled-bunch eigenmodes to a frequency span from DC to  $\omega_{\text{rev}}/2$ . Such a spectrum allows the operator to very quickly check how well the system damps the coupled-bunch motion.

**DATA ACQUISITION CONTROL ON/OFF**

## 5.6 Display Panels

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Data acquisition enable. Turn this control to on to acquire and post-process the data.

### **CONTINUOUS/SINGLE**

Selects between single acquisition mode and continuous updates.

### **MEAN**

Overall mean of the data.

### **RMS**

Overall RMS of the data.

### **AMP P-P**

Peak-to-peak amplitude of the gap transient.

### **MAX RMS**

Largest RMS around the turn.

### **SPECTRUM AVERAGING PATTERN**

Bunch pattern in the format described in Sec. 5.3. This field allows the user to select a subset of bunches for quadratically averaging in the spectrum plot. Using this field one can examine single-bunch spectra or, for example, select only filled buckets to improve signal-to-noise ratio.

### **MARKER SPAN**

Two independent markers allow the user to search for peaks or notches in the spectrum. Lower and upper bounds of a frequency search range in kHz are specified for each marker. Within this frequency range the IOC code searches the averaged spectrum and, based on the search type, finds maximum (peak) or minimum (notch) value and frequency.

### **MIN/MAX**

Spectrum search type: minimum or maximum. Maximum search is used for tracking positive peaks, e.g. in driven tune monitoring or in open loop. When the feedback loop is closed a notch typically forms in the spectrum at the tune frequency. Minimum search can then be used to provide parasitic non-invasive tune readout.

**AVG**

Spectrum averaging constant. Value roughly corresponds to the averaging time constant expressed in spectrum updates. For example, setting this field to 10 produces exponential time constant of 10 seconds at 1 Hz update rate. Value of 1 disables averaging.

**MARKER**

Marker amplitudes in dB.

**FREQ**

Marker frequencies in kHz.

**5.6.11 Single Bunch Acquisition Controls**

The interface is titled "ID=IGPF:TEST:SB" and includes "HELP" and "EXIT" buttons. It is divided into two main sections: "DATA ACQUISITION" and "Waveforms".

**DATA ACQUISITION** parameters:

- ACQUISITION TIME: 15.7 ms
- BUNCH NUMBER: 1
- ACQ SAMPLES: 98304
- CURRENT BUNCH: 0

**Waveforms** section:

- TRIGGER** controls:
  - INT (Internal) and TRIG1 (Trigger 1) buttons.
  - EXT (External) and TRIG2 (Trigger 2) buttons.
- Arm** button with "OFF" status.
- Auto re-arm** button with "OFF" status.
- RESET** button (highlighted in green).

Figure 16: Single bunch acquisition control panel

This panel controls the parameters of the single bunch acquisition engine.

**ACQUISITION TIME**

Acquisition time duration. Maximum acquisition length is defined by the revolution frequency.

**BUNCH NUMBER**

Bunch number (starting from 1) to acquire.

### **ACQ SAMPLES**

Computed acquisition length is reported in this field.

### **CURRENT BUNCH**

Number of the bunch, captured in the last acquisition.

### **Waveforms**

Opens the appropriate waveform display panel.

### **TRIGGER INT/EXT**

Acquisition trigger source, internal or external.

### **TRIG1/TRIG2**

Selects external trigger source input.

### **Arm**

External trigger is only valid if the acquisition system is armed. Single-event acquisitions on the external trigger can be performed by pushing this button.

### **Auto re-arm**

This option re-arms the acquisition system after each data readout. This allows for continuous updates of beam data triggered by external signal. Note that the first acquisition on external trigger must be armed manually.

## 5.6.12 Single Bunch Waveforms Panel

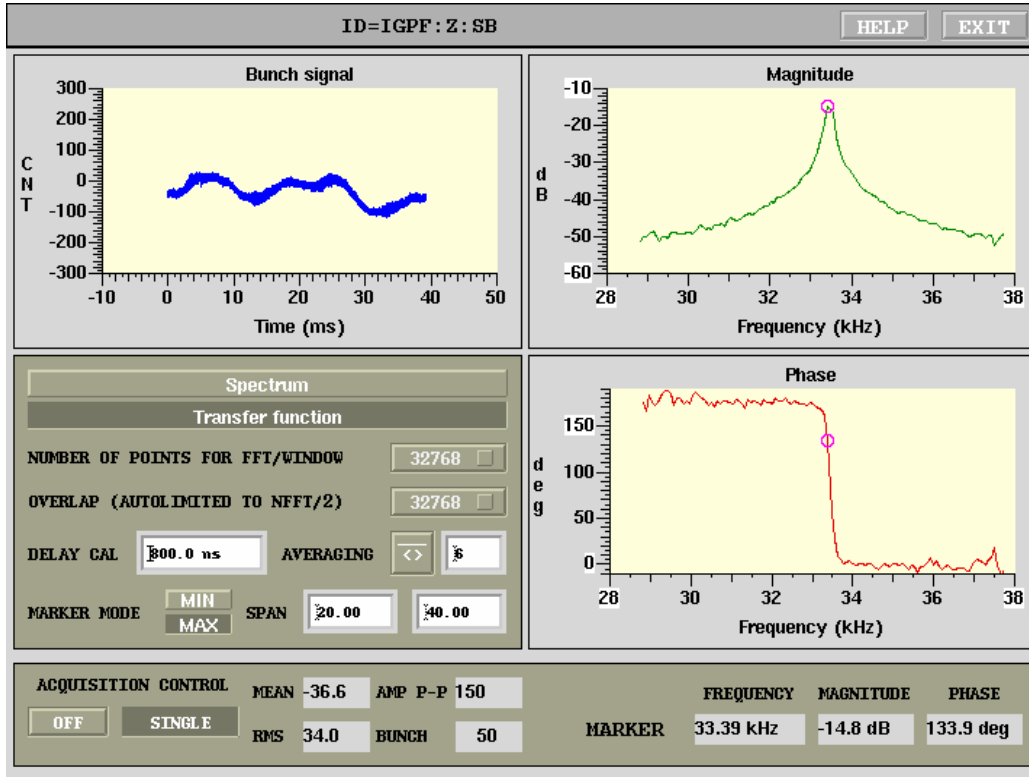


Figure 17: Single bunch waveforms panel

A set of IOC subroutines postprocesses the data in the real-time and generates three plots displayed in the waveform panel shown in Figure 17. The three plots are: time-domain record of bunch motion, frequency-domain magnitude and phase.

Frequency domain plots can operate in two modes: spectrum and transfer function. In the spectrum mode, power spectral density estimate is computed from the raw bunch data using Welch's averaged, modified periodogram method. Data vector is divided into sections, defined by the FFT length, with the overlap up to half the length. Each section is windowed using a Hamming window. FFT spectra are then averaged to obtain the magnitude vector. In the transfer function mode, the IOC computes the excitation waveform  $x$ , then estimates the external transfer function to beam signal  $y$  using

## 5.6 Display Panels

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the quotient of cross power spectral density  $P_{xy}$  and power spectral density of  $x$ ,  $P_{xx}$ .

### **Spectrum/Transfer function**

This control selects between the two frequency domain processing modes, described above. In the spectrum mode, phase plot is disabled. When transfer function mode is selected, plotted frequency range is automatically clipped to the span, covered by the excitation waveform. If the drive waveform sweeping is turned off, transfer function plots are blanked.

### **NFFT**

Selector for the FFT and window length. This defines the frequency resolution.

### **OVERLAP**

Section overlap. This is automatically limited to half of NFFT setting. Can be usually left at the maximum value of 32768.

### **DELAY CAL**

A fixed delay offset can be added to the phase plot, to compensate for physical transport delays between the DAC output and the ADC input.

### **AVERAGING**

Spectrum averaging constant. Value roughly corresponds to the averaging time constant expressed in spectrum updates. For example, setting this field to 10 produces exponential time constant of 10 seconds at 1 Hz update rate. Value of 1 disables averaging.

### **MARKER SPAN**

A marker can be used to search for peaks or notches in the magnitude plot. Lower and upper bounds of a frequency search range in kHz are specified for each marker. Within this frequency range the IOC code searches the averaged spectrum and, based on the search type, finds maximum (peak) or minimum (notch) value and frequency.

### **MIN/MAX**

Spectrum search type: minimum or maximum.

**ACQUISITION CONTROL ON/OFF**

Data acquisition enable. Turn this control to on to acquire and post-process the data.

**CONTINUOUS/SINGLE**

Selects between single acquisition mode and continuous updates.

**MEAN**

Mean of the data.

**RMS**

RMS of the data.

**AMP P-P**

Peak-to-peak amplitude.

**BUNCH**

Bunch number.

**FREQUENCY**

Marker frequency in kHz.

**MAGNITUDE**

Marker magnitude in dB.

**PHASE**

Marker phase in degrees.

**5.6.13 Environmental Monitoring Panel**

The environmental monitoring panel shown in Figure 18 provides instantaneous readouts and five minute histories of five supply voltages and four temperatures in the iGp12-400F system. It also monitors IOC CPU temperature and two cooling fan speeds: one mounted on the IOC CPU and the main chassis fan.

**NOTE:** *The user must check the device temperatures after the unit is installed in the final location to make sure sufficient airflow reaches the internal devices.*

## 5.6 Display Panels

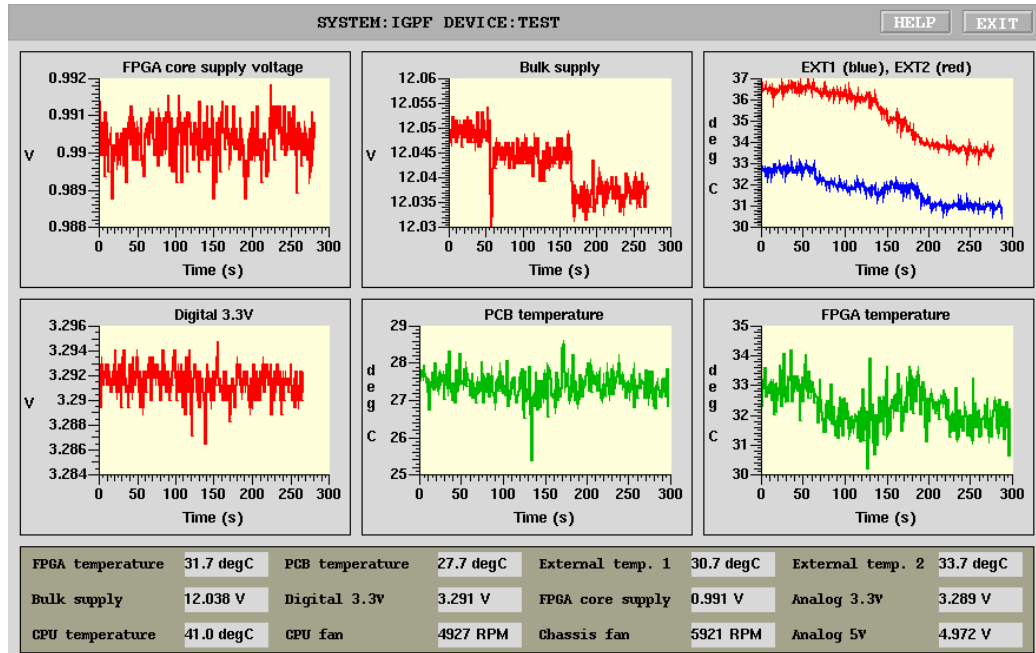


Figure 18: Environmental monitoring panel

**NOTE:** Check device temperatures periodically and compare to measurements made during installation. Elevated temperatures can indicate blocked air intake filter!

The iGp12-400F can continue operating with the main chassis fan stopped, however such operation puts high stress on certain key semiconductor devices. Prolonged operation with non-functional main chassis fan should be avoided.

### 5.6.14 Device Controls Panel

Device controls panel provides control interface to several peripherals integrated in the iGp12-400F. There are four adjustable delay units for controlling the high-speed ADC, DAC, and fiducial timing.

**WARNING:** While these delay controls can be used to adjust various clock timings, one is strongly advised to perform the adjustments via the timing panel. Timing panel controls interface to a



**ID=IGPF:TEST** HELP EXIT

DELAY LINES		THRESHOLDS AND OFFSETS	
ADC CLOCK	50	FIDUCIAL	STD 400.0 mV
FIDUCIAL CLOCK	96	TRIGGER 1	STD 1650.0 mV
FIDUCIAL	182	TRIGGER 2	STD 1420.0 mV
DAC CLOCK	0	DAC OFFSET	0.00 mV

SHAPER FIR ([C0 2<sup>17</sup> C2])    C0 0    C2 0

AD5644 DACs  
MAX1202 ADC  
GPIO  
TIMING  
POWER AMPS  
MASKS  
INFO

Figure 19: Device controls panel

sophisticated IOC routine which in turn computes the necessary settings of the four delay units.

Thresholds and offsets area is dedicated to adjusting logic level thresholds for the fiducial and trigger inputs. Three control elements are provided for each signal. STD/ARB selects between a pre-defined signal standard or an arbitrary threshold. In the arbitrary threshold mode, a value in the range of  $\pm 3000$  millivolts can be entered to the right of the selector. When standard mode is selected, threshold value is determined by the menu selection on the left. Available standards include NO DC, NIM, emitter coupled logic (ECL), LVPECL, LVDS, LVTTTL, and TTL/2 (0 to 2.5 V).

For two external triggers one can select the active edge — rising or falling. Internally this is implemented as inversion of the trigger signal before it is delivered to the acquisition units. Thus, trigger level capture in SRAM and BRAM is sensitive to these two settings.

DAC OFFSET field is used to trim the DC offset of the high-speed DAC. This value is configured at the factory and should not need adjustment.

FPGA gateway for iGp12 includes a 3-tap output shaper FIR. Out of three coefficients ( $C_0$ ,  $C_1$ ,  $C_2$ ), central coefficient  $C_1$  is fixed at unity ( $2^{17}$  full scale), with the other two adjustable in the range from  $(-2^{17} + 1)$  to  $(2^{17} - 1)$ .

## 5.6 Display Panels

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By adjusting  $C_0$  and  $C_2$  one can pre-distort the DAC output to compensate for the response of the back-end section (power amplifier, kicker).

From the device control panel one can open the following seven panels:

- AD5644 DACs, section 5.6.16;
- MAX1202 ADC, section 5.6.17;
- GPIO, section 5.6.18;
- TIMING, section 5.6.6;
- POWER AMPS, section 5.6.19;
- MASKS, section 5.6.15;
- INFO, section 5.6.23.

### 5.6.15 Mask Panel

This panel allows the user to quickly examine bunch-by-bunch enable masks for feedback, drive, and spectral averaging. When generated from the appropriate pattern strings these correspond directly to the user's specification. However one can also use channel access to directly set these masks. Mask display panel allows one to verify that the actual masks are in agreement with the expected patterns.

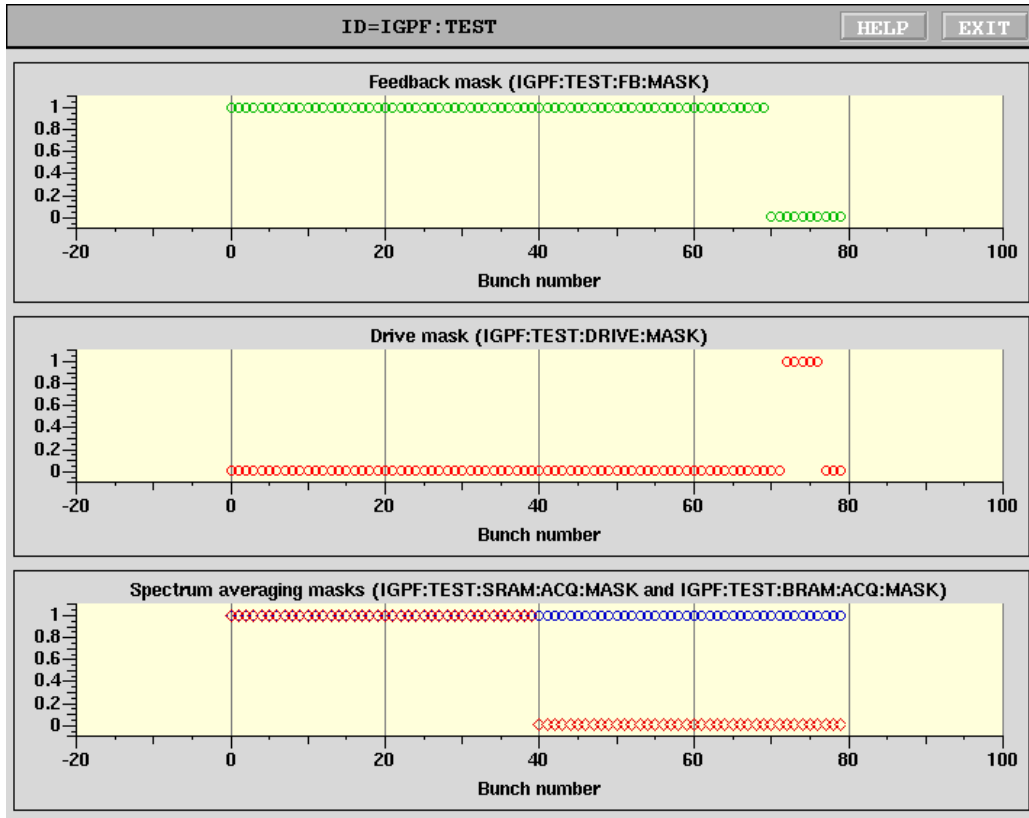


Figure 20: Bunch enable masks panel

### 5.6.16 AD5644 8-channel DAC Panel

Eight general-purpose DAC outputs are controlled from this panel. Each output has 14-bit resolution with  $\pm 3$  V drive capability into high impedance. With  $50\ \Omega$  loads the output levels are reduced by a factor of 2.

Reference selection and test mode switch are reserved for factory testing.

### 5.6.17 MAX1202 8-channel ADC Panel

This panel provides readouts of the eight 12-bit ADC channels updated at 1 Hz. The input signals are low-pass filtered to 1 kHz before sampling.

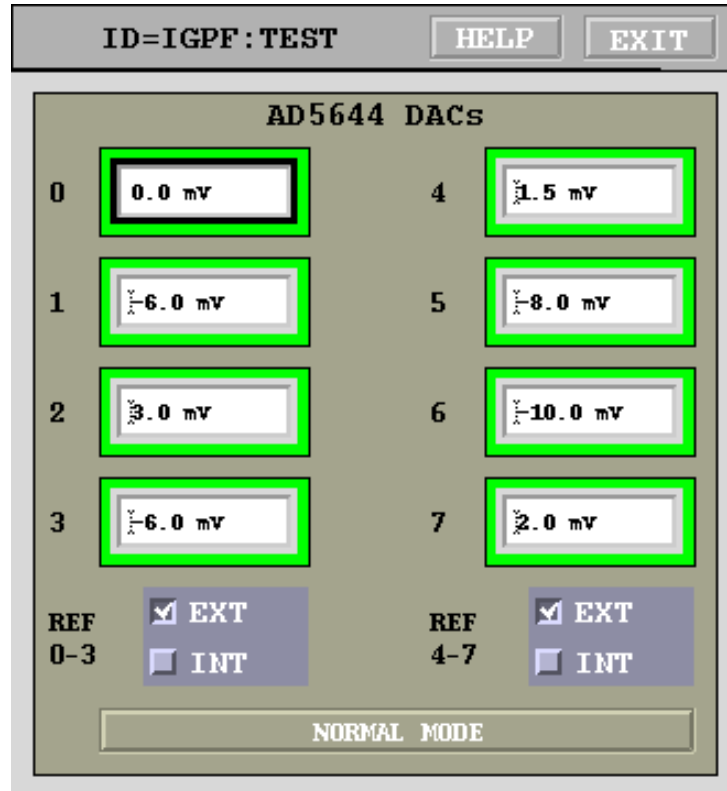


Figure 21: 8-channel DAC panel

#### 5.6.18 GPIO Panels

General-purpose I/O control panel consists of three different panels, one for bit-by-bit GPIO, one for the single-channel front/back-end (FBE), and one for the three-channel front/back-end (FBE-LT). Using the choice buttons on the top of the panel one can select one of the three drivers. Selected driver is connected to the GPIO pins and the appropriate panel is displayed in the window.

**WARNING:** Front/back-end drivers set several I/O pins as outputs. Make sure correct hardware is connected to the GPIO port before selecting these drivers! Improper driver selection may cause damage to the output pins and the connected external devices.

Bit-by-bit control panel, shown in Figure 23 provides individual bit controls for 32 LVTTL signals available on the rear panel. Each bit control in-

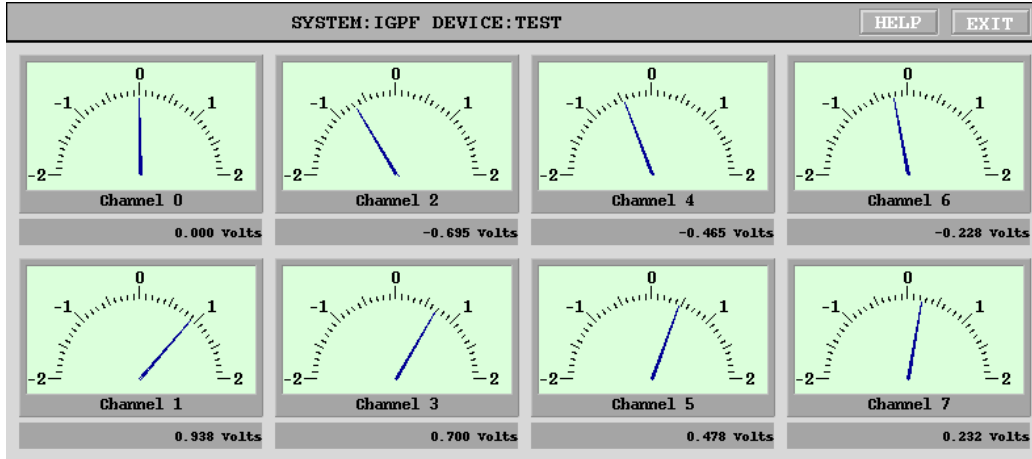


Figure 22: 8-channel ADC panel

cludes output value (0 or 1), direction (In or Out), and the readback. When the signal is configured for output the readback should reflect the output value.

Figure 24 shows the front/back-end panel. This panel is split into two portions: front/back-end registers and the phase servo loop. The register controls include front and back-end phase and attenuation. Phase adjustments are performed using a 12-bit DAC with the allowed control range from 0 to 4095. Front-end phase register setting is provided as a readout labeled FRONT-END PHASE DAC SETTING. When the phase servo loop is open the register is directly driven by the front-end phase control setpoint. Closed phase servo loop adjusts the register value around the setpoint to center the ADC signal. Front and back-end attenuation settings adjust digital attenuators in steps of 0.5 dB. Control values are in dB and are rounded automatically. Full adjustment range is from 0 to 31.5 dB.

Phase servo loop can be closed and opened by the LOOP CLOSURE buttons. Depending on which zero crossing the phase shifter is centered different loop polarities need to be selected using LOOP SIGN. LOOP GAIN parameter must be adjusted to optimize the loop response in terms of noise, bandwidth, and overshoot. Typically the optimization can be carried out with beam by stepping the input offset and observing the phase servo response using a stripchart tool. INPUT OFFSET is used to zero out possible

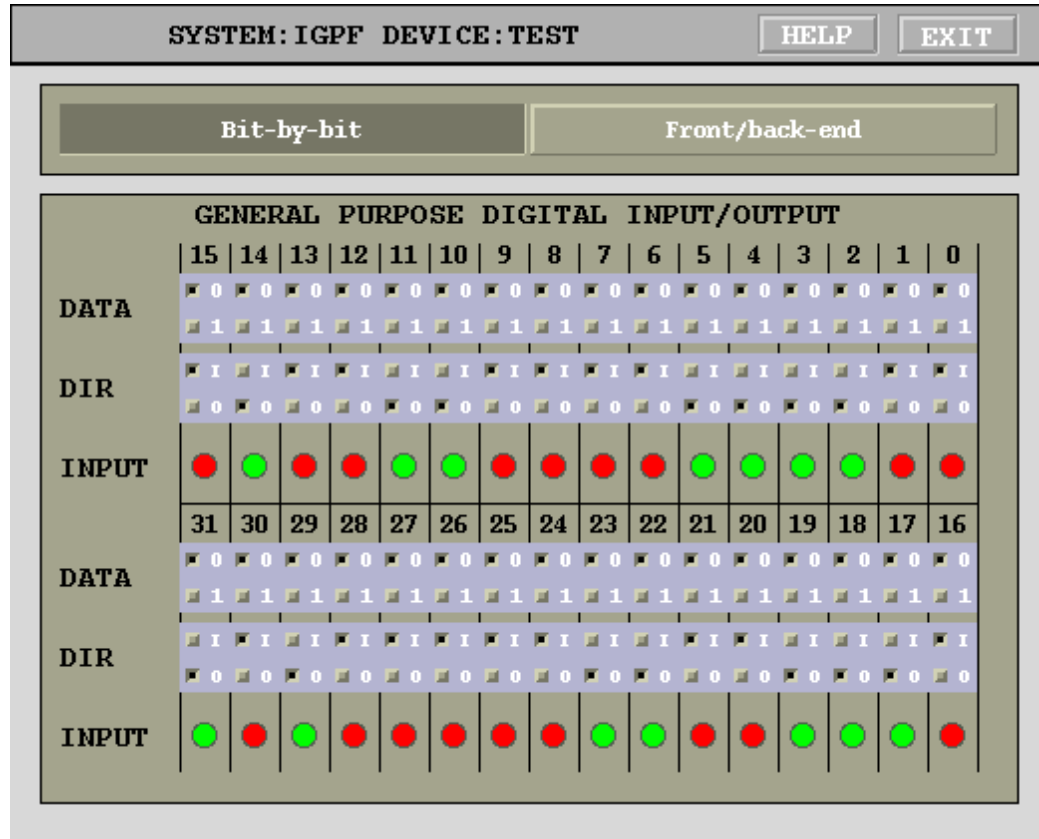


Figure 23: General-purpose I/O panel: bit-by-bit driver

mixer offset or, alternatively, to introduce an offset. Such an offset is typically used when the beam loading transient is highly asymmetric to avoid reaching ADC saturation prematurely. SATURATION LIMIT parameter defines the maximum deviation from the phase setpoint that can be introduced by the phase servo. This limit must be set below  $\pi/2$  to make sure the phase servo does not transition from one zero crossing to another.

Readouts on the bottom provide information on the ADC input offset and the phase servo output. The bar indicator and the readout on the left show the output of a Cascaded Integrator Comb (CIC) decimator which averages  $10^9$  input samples (0.22 Hz  $-3$  dB bandwidth). The indicator on the right shows the phase servo correction applied to the setpoint. This indication

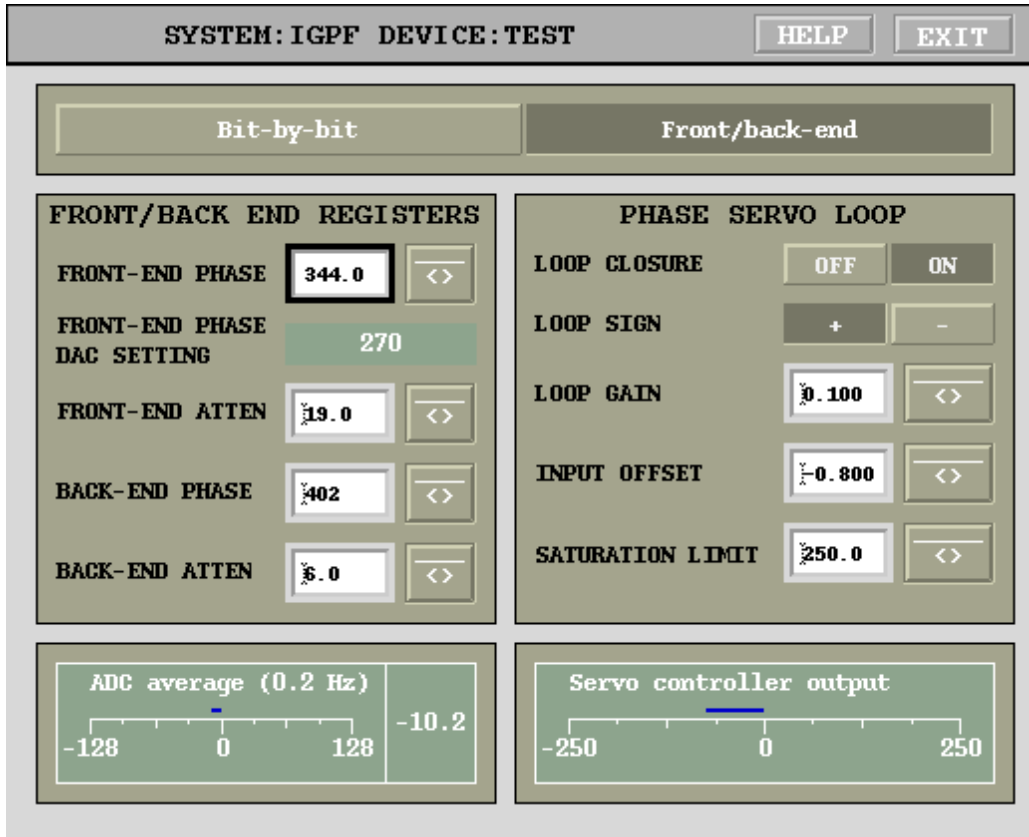


Figure 24: General-purpose I/O panel: front/back-end driver

can be used to adjust the setpoint for near-zero correction. Such near-zero correction is optimal for closed/open phase servo loop transitions and for low beam current operation.

Panel for the all-axis front/back-end (FBE-LT) is shown in Fig. 25. FBE-LT has three front-end channels and one back-end channel. Each channel has an attenuator and a carrier phase shifter. Channels are labeled as horizontal, vertical, and longitudinal. Attenuator and phase shifter controls are identical to those described above for the FBE driver.

Since the phase servo loop needs to measure the longitudinal ADC and then to adjust the longitudinal phase shifter, FBE-LT should be connected to the longitudinal iGp12-400F.

## 5.6 Display Panels

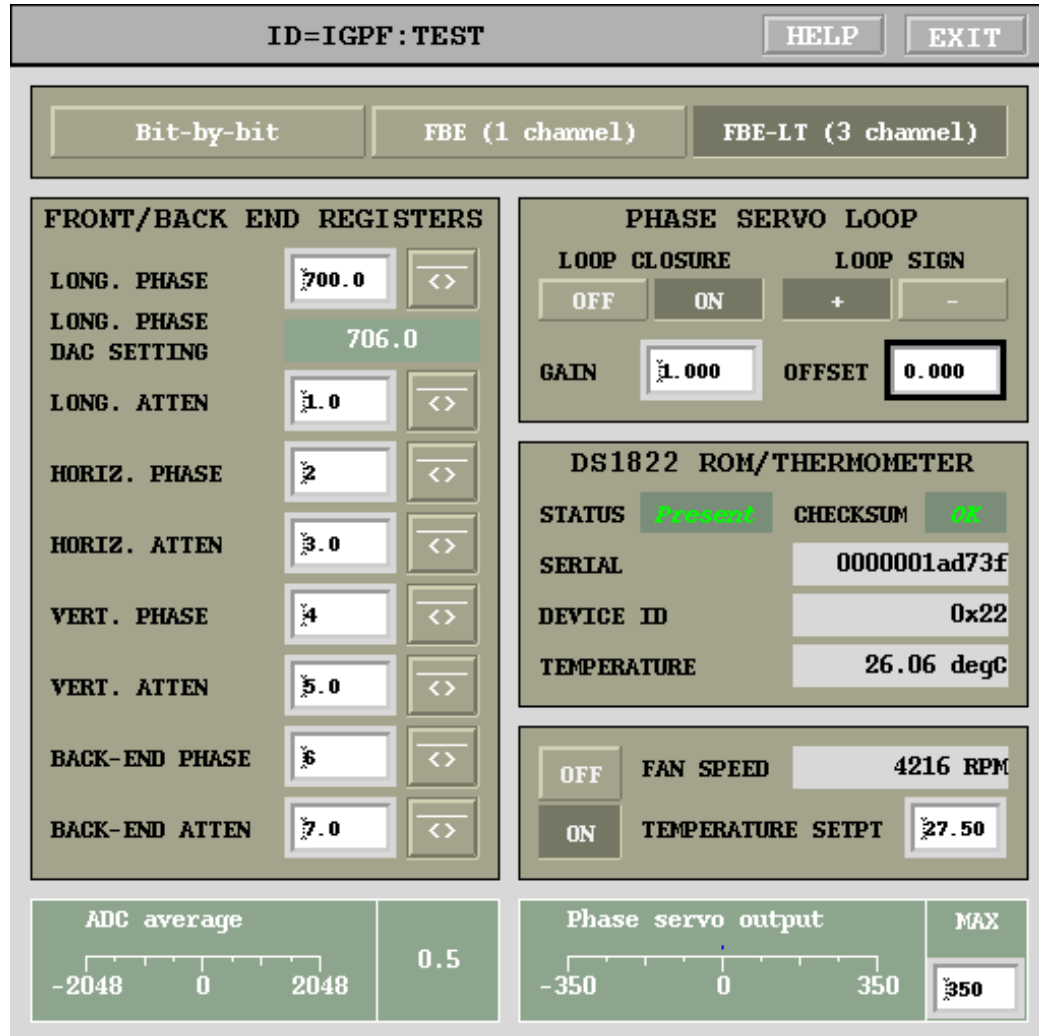


Figure 25: General-purpose I/O panel: FBE-LT driver

FBE-LT integrates a Maxim DS1822 device which provides a unique serial number as well as temperature monitoring. DS1822 status and checksum should read *present* and *OK* when FBE-LT is connected and the appropriate driver is selected.

Interface between iGp12-400F and FBE-LT also allows control and monitoring of the FBE-LT cooling fan. Fan speed is displayed in RPM. Speed



control can operate in two modes: open and closed-loop. In the open-loop mode the fan is set to the maximum speed. In the closed-loop mode a proportional integral (PI) controller adjusts the fan speed to maintain the temperature, measured by DS1822, close to the temperature setpoint. This temperature control method is limited by the ambient temperature at the low end and the still-air device temperature. Selecting too low a setpoint can result in positive temperature errors with the fan running at the maximum speed. Similarly, too high a setpoint can generate negative temperature errors at the minimum fan speed.

When selecting the temperature setpoint one should collect data on the system temperature with the loop open over several days. Select a setpoint higher than the maximum temperature observed in this experiment. Observe closed-loop operation and raise the setpoint if the ambient temperature swings cause the unit to run hot. The goal is to use the lowest possible setpoint while still maintaining temperature regulation.

#### 5.6.19 Power Amplifiers Panel

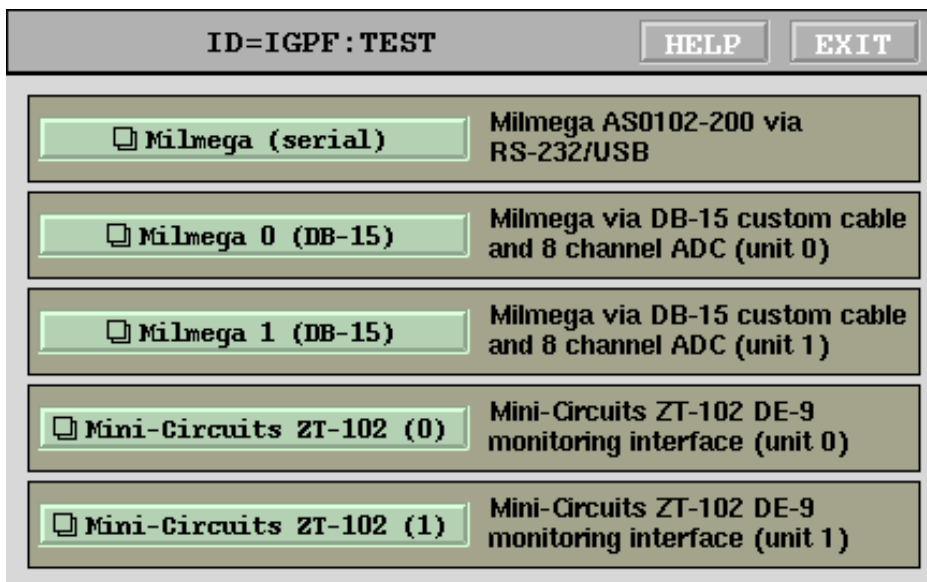


Figure 26: Power amplifiers panel

Several power amplifier interfaces are supported by iGp12-400F. Control and readout panels for these are collected in the power amplifiers panel shown

## 5.6 Display Panels

in Fig. 26. The first panel allows to control MILMEGA power amplifiers (AS0102-200 and AS0102-250) via USB or serial connection. The amplifier must be connected to iGp12-400F prior to running setup script, which detects the amplifier and configures the interface appropriately. Next, there are two panels for monitoring two MILMEGA amplifiers via rear-panel DB-15 connector. Custom cable can be provided by Dimtel, Inc. to connect two amplifiers to the 8-channel ADC port of iGp12-400F. Finally, there are two panels for monitoring two Mini-Circuits ZT-102 power amplifiers. These are monitored by the 8-channel ADC and require a special cable.

### 5.6.20 MILMEGA serial/USB

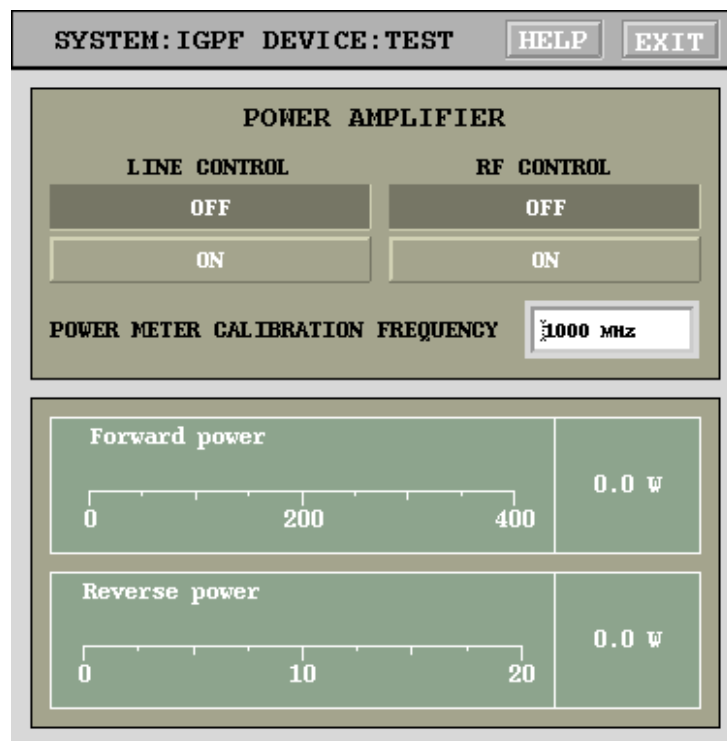


Figure 27: MILMEGA amplifier control and monitoring panel (serial/USB)

iGp12-400F IOC includes driver support for MILMEGA power amplifier, models AS0102-200 and AS0102-250. IOC can communicate with the amplifier via USB or RS-232 serial port. Control and monitoring functions

are combined on the power amplifier panel shown in Fig. 28. Two control functions are available: line and RF. Line power switch turns main power supply on and off. That also controls the state of the cooling fans. RF control enables actual amplifier operation. Both controls will show inconsistencies between EPICS setting and amplifier readback in magenta. Two power meter readings are monitored at 1 Hz: forward and reverse power. Internally, Milmega amplifiers store calibration tables for these power monitors. POWER METER CALIBRATION FREQUENCY setting allows the user to select calibration value appropriate for the output frequency used.

#### 5.6.21 MILMEGA DB-15

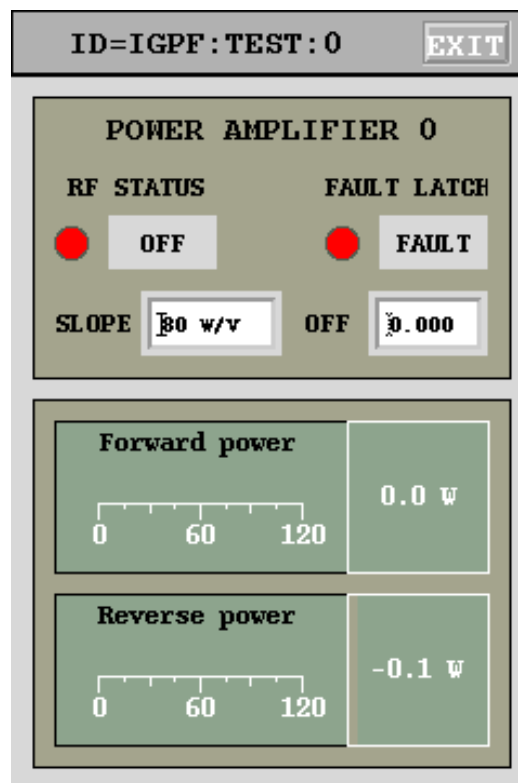


Figure 28: MILMEGA amplifier monitoring panel (DB-15)

These panels are configured to monitor four parameters each on two MILMEGA amplifiers. RF status and fault latch are monitored, as well

## 5.6 Display Panels

as forward and reflected power. For proper readout of the power levels, calibration of slope and offset parameters is needed.

### 5.6.22 Mini-Circuits ZT-102

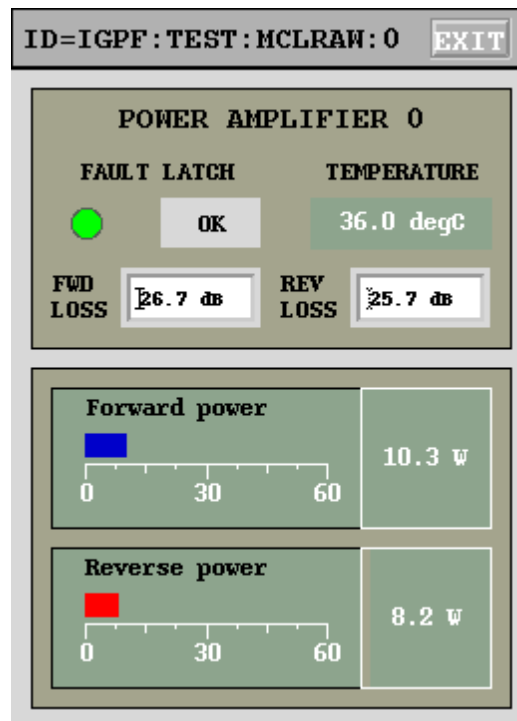


Figure 29: Mini-Circuits ZT-102 monitoring via DE-9 front panel connector

These panels are configured to monitor four parameters each on two Mini-Circuits ZT-102 amplifiers. Fault output and internal temperature are monitored, as well as forward and reflected power. For proper readout of the power levels, directional coupler loss factors need to be calibrated.

### 5.6.23 Information Panel

Information panel summarizes some system configuration parameters. Harmonic number, gateway revision, and gateway type are read from the FPGA configuration register during IOC startup. These values are used to look-up

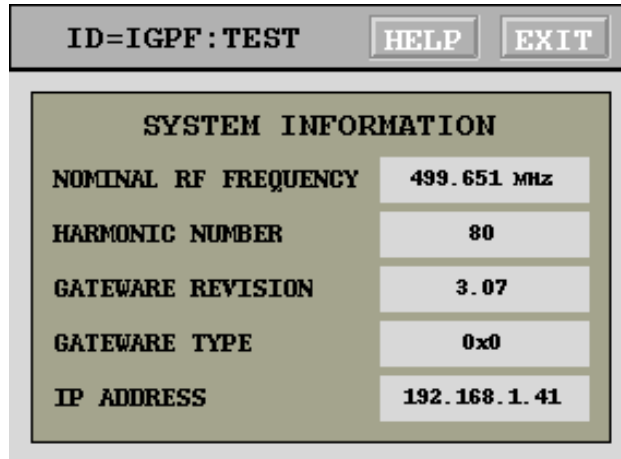


Figure 30: Information panel

the appropriate accelerator in an internal table and to select the nominal RF frequency. IP address of the IOC is also displayed.

## 6 External Software Interface

Software distribution CD includes several tools extract iGp12-400F data for analysis and processing in external software programs. These tools are written for MATLAB® and use LabCA package for communicating with EPICS.

### iGp\_read

Top-level data acquisition tool. This script will read out data from the iGp12-400F, create a timestamped directory, and save the data in a file called `gd.mat`. This file is in a format, compatible with MATLAB® data analysis tools, developed for ALS/LNF-INFN/SLAC longitudinal feedback systems.

### get\_data

This function reads out the raw data vector from the IOC and returns it to the caller. A single argument is the PV root name, e.g. `IGPF:TEST:`.

### adctest

This function extracts the iGp12-400F data and fits a sinewave to it. It accepts the IOC device name and the number of times to repeat the acquisition/fitting cycle.

## 7 Specifications

**Table 2: General specifications**

Parameter	Definition
Operating frequency	499.66 MHz
RF input level	−9 to 9 dBm, -3 dBm nominal
Number of FIR taps	32
Harmonic number	400
Fiducial signal	Falling edge trigger, selectable threshold
Minimum fiducial pulse width	2 ns
External trigger inputs	2 inputs, rising/falling edge, selectable threshold
Minimum trigger pulse width	2 ns
Data acquisition memory (SRAM)	12 Msamples
FPGA dual-port memory (blockRAM)	276 ksamples
Slow analog inputs	8 channels @12 bits, -2.048 to 2.048 V
Slow analog outputs	8 channels @14 bits, −1.5 to 1.5 V swing into 50 $\Omega$
General purpose digital I/O	32 bits in/out, LVTTL
Chassis	2U 19" rackmount, 16" deep

**Table 3: High-speed ADC and DAC specifications**

Parameter	Definition
ADC inputs	2 complementary
ADC input impedance	50 $\Omega$
ADC input full scale sensitivity	780 mV peak-to-peak (+1.8 dBm)
ADC resolution	12 bits
ADC input bandwidth	1.3 GHz
DAC outputs	2 complementary
DAC output impedance	50 $\Omega$
DAC FS	800 mV peak-to-peak (+2 dBm)
DAC resolution	12 bits
DAC rise time (10%-90% FS)	350 ps
DAC fall time (90%-10% FS)	350 ps

**Table 4: Trigger and fiducial inputs**

Parameter	Definition
Minimum input level	-3.3 V
Maximum input level	3.3 V
Termination impedance	50 $\Omega$
Switching threshold range	$\pm 3$ V
Minimum high level	-1.3 V
Maximum low level	3.1 V
Minimum swing (input to threshold)	0.2 V
Maximum swing (input to threshold)	4.3 V

**Table 5: FIR filter control**

Parameter	Definition
Coefficients	16 bit wide in Q15 format
Coefficient sets	2
Coefficient set select	0 or 1
FIR channel enable control	On/Off
Shift gain	0 to 7
Downsampling	1 to 32

**Table 6: Control parameters**

Parameter	Definition
One-turn delay adjustment	$T_{\text{RF}}$ per step, up to one revolution
DCM reset	Control panel pushbutton
Clock and fiducial delays	4 channels
Clock and fiducial delay step	10 ps
Clock and fiducial delay range	0–10.23 ns
General-purpose analog outputs	8 channels
Fiducial and trigger thresholds	3 channels
High-speed DAC offset adjustment	1 channel
General-purpose digital outputs	32 inputs/outputs

**Table 7: Data acquisition controls**

Parameter	Definition
Recording memory selection	FPGA internal blockRAM or external SRAM
Measurement trigger	Internal or external
External trigger arming	Single or after every beam data read-out
Recorded growth length	Adjustable in units of 3 samples, up to full memory length
Hold-off before recording	In units of 3 samples, 0 to $2^{32} - 1$
Recording downsampling	1 to 32

**Table 8: Monitoring and diagnostics**

Parameter	Definition
Clock status	RF clock missing, DCM lock
Feedback channel status	FIR saturation
Acquisition state machine status	Trigger arming bit
Voltages	FPGA core supply, 3.3 V, 5 V, 12 V bulk
Temperatures	FPGA, ambient, two ECL devices
Analog inputs	8 slow ADC channels
Digital inputs	32 general-purpose inputs/outputs



**Table 9: Drive pattern generator**

Parameter	Definition
Output waveform	Sine, square, or DC
Amplitude	0–1
Bunch selectability	Bunch-by-bunch drive enable mask. Allows any subset of bunches to be driven
Frequency range	$0-F_{\text{rf}}/2$

**Table 10: Input Power Requirements**

Parameter	Definition
Input voltage	115/230 VAC
Input current	2/1 A
Frequency	60/50 Hz
Voltage selection	Switch
Low voltage range	104–126 V
High voltage range	207–253 V

## 8 Warranty and Support

### 8.1 Warranty

Dintel Inc. warrants this product for a period of one year from the date of shipment against defective workmanship or materials. This warranty excludes any defects, failures or damage caused by improper use or inadequate maintenance, installation or repair performed by Customer or a third party not authorized by Dintel, Inc. Warrantied goods will be either repaired or replaced at the discretion of Dintel, Inc. The above warranties are exclusive and no other warranty, whether written or oral, is expressed or implied.

### 8.2 Support

Dintel Inc. will provide technical support for the product free of charge for a period of one year from the date of shipment. Such support is defined to include:

- FPGA gateware bug fixes and upgrades;
- IOC software bug fixes and upgrades;
- Client software (display panels, external interface) bug fixes and upgrades;
- Phone, e-mail, and remote access (when allowed by the Customer) support of software and hardware integration.

Free of charge technical support specifically excludes:

- Commissioning with beam;
- Feedback algorithm development and testing;
- Beam dynamics characterization;
- Operational support related to dynamic system operation.

## 9 Appendix A: Address Map

### 9.1 Registers

#### 9.1.1 Overall Layout

The general register layout for the iGp12-400F reserves space below 0x100 for FIR coefficients. This allows for a maximum of 128 coefficients in two sets. Control and status registers are placed starting at 0x100.

Table 11: FPGA registers: FIR

Address	Bits	Definition
0x000000	15:0	FIR coefficient 0, set 0
0x000001	15:0	FIR coefficient 0, set 1
0x000002	15:0	FIR coefficient 1, set 0
0x000003	15:0	FIR coefficient 1, set 1
0x000004	15:0	FIR coefficient 2, set 0
0x000005	15:0	FIR coefficient 2, set 1
0x000006	15:0	FIR coefficient 3, set 0
0x000007	15:0	FIR coefficient 3, set 1
0x000008	15:0	FIR coefficient 4, set 0
0x000009	15:0	FIR coefficient 4, set 1
0x00000a	15:0	FIR coefficient 5, set 0
0x00000b	15:0	FIR coefficient 5, set 1
0x00000c	15:0	FIR coefficient 6, set 0
0x00000d	15:0	FIR coefficient 6, set 1
0x00000e	15:0	FIR coefficient 7, set 0
0x00000f	15:0	FIR coefficient 7, set 1
0x000010	15:0	FIR coefficient 8, set 0
0x000011	15:0	FIR coefficient 8, set 1
0x000012	15:0	FIR coefficient 9, set 0
0x000013	15:0	FIR coefficient 9, set 1
0x000014	15:0	FIR coefficient 10, set 0
0x000015	15:0	FIR coefficient 10, set 1
0x000016	15:0	FIR coefficient 11, set 0
0x000017	15:0	FIR coefficient 11, set 1
Continued on next page		

Table 11 – continued from previous page

Address	Bits	Definition
0x000018	15:0	FIR coefficient 12, set 0
0x000019	15:0	FIR coefficient 12, set 1
0x00001a	15:0	FIR coefficient 13, set 0
0x00001b	15:0	FIR coefficient 13, set 1
0x00001c	15:0	FIR coefficient 14, set 0
0x00001d	15:0	FIR coefficient 14, set 1
0x00001e	15:0	FIR coefficient 15, set 0
0x00001f	15:0	FIR coefficient 15, set 1
0x000020	15:0	FIR coefficient 16, set 0
0x000021	15:0	FIR coefficient 15, set 1
0x000022	15:0	FIR coefficient 17, set 0
0x000023	15:0	FIR coefficient 17, set 1
0x000024	15:0	FIR coefficient 18, set 0
0x000025	15:0	FIR coefficient 18, set 1
0x000026	15:0	FIR coefficient 19, set 0
0x000027	15:0	FIR coefficient 19, set 1
0x000028	15:0	FIR coefficient 20, set 0
0x000029	15:0	FIR coefficient 20, set 1
0x00002a	15:0	FIR coefficient 21, set 0
0x00002b	15:0	FIR coefficient 21, set 1
0x00002c	15:0	FIR coefficient 22, set 0
0x00002d	15:0	FIR coefficient 22, set 1
0x00002e	15:0	FIR coefficient 23, set 0
0x00002f	15:0	FIR coefficient 23, set 1
0x000030	15:0	FIR coefficient 24, set 0
0x000031	15:0	FIR coefficient 24, set 1
0x000032	15:0	FIR coefficient 25, set 0
0x000033	15:0	FIR coefficient 25, set 1
0x000034	15:0	FIR coefficient 26, set 0
0x000035	15:0	FIR coefficient 26, set 1
0x000036	15:0	FIR coefficient 27, set 0
0x000037	15:0	FIR coefficient 27, set 1
0x000038	15:0	FIR coefficient 28, set 0
0x000039	15:0	FIR coefficient 28, set 1
0x00003a	15:0	FIR coefficient 29, set 0
Continued on next page		

Table 11 – continued from previous page

Address	Bits	Definition
0x00003b	15:0	FIR coefficient 29, set 1
0x00003c	15:0	FIR coefficient 30, set 0
0x00003d	15:0	FIR coefficient 30, set 1
0x00003e	15:0	FIR coefficient 31, set 0
0x00003f	15:0	FIR coefficient 31, set 1

### 9.1.2 Gateway Config Register

Gateway configuration register (0x107) provides information about the unit's functionality, gateway revision, harmonic number, and processing demultiplexing.

Table 12: FPGA registers: control and status

Address	Bits	Definition
0x000100	Main control register	
	0	Data acquisition trigger
	1	External trigger input select, 1 - TRIG1, 0 - TRIG2
	2	Coefficient set select, 0 - set 0, 1 - set 1
	3	FIR channel disable, 1 - disabled
	6:4	Shift gain, 0 through 7
	7	DCM reset
	8	Grow/damp enable
	9	Trigger select, 1 - external
	10	External trigger arming, arms on rising edge
	11	SRAM interface select, 0 - local bus, 1 - ADC
	12	ADC test pattern generator enable
	13	DAC drive phase: 0 - 0 degrees, 1 - 180 degrees
	15:14	Reserved
	16	GPIO driver select, 0 - bit-by-bit, 1 - FBE
	31-17	Reserved
Continued on next page		

Table 12 – continued from previous page

Address	Bits	Definition
0x000101	Status register, reset on read	
	0	RF clock missing
	1	Saturation
	2	Processing DCM unlocked
	3	External trigger arming status
	4	Local bus clock DCM unlocked
	5	Fiducial error
	6	Acquisition DCM unlocked
	7	ADC over-range
	31:8	Reserved
0x000102	DCM phase shift register	
	8:0	Phase shift, signed 9-bit value from -256 ( $-2\pi$ ) to 255 ( $2\pi$ )
	31:9	Unused, read out as 0
0x000104	Output delay length	
	10:0	Delay length in units of 4 samples
	15:11	Recording downsampling, 0 - every turn, $N_{ds} = \text{regval} + 1$
	20:16	Processing downsampling
	27:24	Fine delay adjustment, one sample per step (larger values produce smaller delay)
	31:28	Reserved
0x000105	Grow/damp filter 2 length	
	21:0	Number of 3-sample groups to hold <i>setsel</i> inverted during data acquisition (growth length)
	31:22	Reserved
Continued on next page		

Table 12 – continued from previous page

Address	Bits	Definition
0x000106	Hold-off length	
	31:0	Number of 3-sample groups to hold <i>setsel</i> inverted before data acquisition
0x000107	Gateway config register (read-only)	
	12:0	Harmonic number
	14:13	Demux mode, 0 - by4, 1 - by6, 2 - by8, 3 - uneven stepping
	15	Reserved
	23:16	Gateway revision
	31:24	Gateway functionality, 0 - feedback
0x000108	Fiducial delay	
	11:0	Fiducial delay, two samples per step
	31:12	Reserved
0x000109	Acquisition length	
	21:0	Acquisition length in units of 3 samples
	31:22	Reserved
0x000200	Acquisition status (read-only)	
	0	Acquisition completed flag
	31:1	Reserved
0x000201	ADC test counter start <sup>1</sup>	
	31:0	Test pattern start value
0x000202	CIC mean output (read-only) <sup>2</sup>	
	31:0	Decimated input average, direct current (DC) gain of $15.625 \times 10^6$

## 9.2 Environmental monitor

iGp12-400F uses two MAX1299 devices for monitoring five temperatures and three power supply voltages. The SPI interface module for the controller uses sixteen addresses, as described in table 13.

<sup>1</sup>Gateway revision 1.2 and higher

<sup>2</sup>Gateway revision 1.4 and higher

## 9.2 Environmental monitor

Let's consider the first device (addresses 0x110–0x117). Analog inputs 0 and 1 (AIN0, AIN1) are connected to the FPGA temperature diode. General conversion function from the raw register value to temperature in degrees Celsius is  $x/32 - 273.15$ . Analog inputs 2 and 3 are used to measure analog 3.3 and 5 V supplies.

MAX1299 also measures the ambient chassis temperature via the internal diode.

Four supply voltages are measured: analog 5 V on AIN2, analog 3.3 V on AIN3, and FPGA core (1 V) is connected to AIN4. Digital 3.3 V supply internally measured by MAX1299. Raw register value can be converted to voltage by  $2.4 \times X / 16384$ . For the 3.3 V supply the value must be multiplied by 4, since MAX1299 monitors  $V_{dd}/4$ . Attenuation factor for the analog 3.3 V supply is 2/3.3 and for the analog 5 V supply it is 2/5.

The second device is configured for external temperature sensors at AIN0–AIN1 and AIN2–AIN3. AIN4 is connected to a resistive divider monitoring bulk 12 V supply. Divider ratio is 1/6 for 2 V nominal ADC input.

Table 13: FPGA registers: MAX1299 monitors

Address	Bits	Definition
0x000110	15:0	Device 1, AIN2 (analog 5 V)
0x000111	15:0	Device 1, AIN3 (analog 3.3 V)
0x000112	15:0	Device 1, AIN4, FPGA core voltage $V_{int}$
0x000113	15:0	Device 1, Internal diode
0x000114	15:0	Device 1, $V_{dd}/4$ , 3.3 V supply monitor
0x000115	15:0	Device 1, External diode (AIN0/AIN1), FPGA die temperature
0x000116	15:0	Device 1, AIN2-AIN3 differential measurement
0x000117	15:0	Device 1, AIN5-AIN5 differential measurement
0x000118	15:0	Device 2, AIN2
0x000119	15:0	Device 2, AIN3
0x00011a	15:0	Device 2, AIN4, bulk supply monitor
0x00011b	15:0	Device 2, Internal diode
0x00011c	15:0	Device 2, $V_{dd}/4$ , 3.3 V supply monitor
0x00011d	15:0	Device 2, External diode (AIN0/AIN1)
0x00011e	15:0	Device 2, External diode (AIN2/AIN3)
Continued on next page		



Table 13 – continued from previous page

Address	Bits	Definition
0x00011f	15:0	Device 2, AIN5-AIN5 differential measurement

### 9.3 MAX1202 8-channel ADC

iGp12-400F includes an 8-channel 12-bit serial-interface ADC. The SPI controller for the ADC uses 8 consecutive addresses, as shown in Table 14. ADC is continuously polled by the controller. Reading one of the channel registers returns the result of the last conversion. ADC data is sign extended from 12 bits to 16. The valid data range is from 0xf800 to 0x7fff. ADC input range is from  $-2.048$  to  $2.047$  V, i.e. 1 mV per LSB.

Table 14: FPGA registers: MAX1202 ADC

Address	Bits	Definition
0x000120	11:0	ADC channel 0
0x000121	11:0	ADC channel 1
0x000122	11:0	ADC channel 2
0x000123	11:0	ADC channel 3
0x000124	11:0	ADC channel 4
0x000125	11:0	ADC channel 5
0x000126	11:0	ADC channel 6
0x000127	11:0	ADC channel 7

### 9.4 AD5644 DACs

iGp12-400F has 3 4-channel 14-bit serial-interface DACs. The SPI controller for the DACs uses 16 consecutive addresses, as shown in Table 15. Writing to one of the registers starts an SPI writing cycle which loads the new value into the DAC. Register reads are sign-extended to 32 bits. Eight outputs are brought out to the front panel, while the remaining four are used to set logic thresholds and trim high-speed DAC. DAC reference voltage is 3 V for  $-3$  to

## 9.5 ECL delay lines

+3 V output range. Output drivers generate full swing into high-impedance loads. For 50  $\Omega$  loads the swing is reduced to 1.5 V.

Table 15: FPGA registers: AD5644 DAC s

Address	Bits	Definition
0x000150	13:0	DAC channel 0
0x000151	13:0	DAC channel 1
0x000152	13:0	DAC channel 2
0x000153	13:0	DAC channel 3
0x000154	13:0	DAC channel 4
0x000155	13:0	DAC channel 5
0x000156	13:0	DAC channel 6
0x000157	13:0	DAC channel 7
0x000158	13:0	DAC channel 8 (TRIG2 threshold)
0x000159	13:0	DAC channel 9 (FID threshold)
0x00015a	13:0	DAC channel 10 (TRIG1 threshold)
0x00015b	13:0	DAC channel 11 (DAC offset)
0x00015c	0	Internal/external reference select, channels 0–3
0x00015d	0	Internal/external reference select, channels 4–7
0x00015e	0	Internal/external reference select, channels 8–11
0x00015f	0	Test mode (sawtooth)

## 9.5 ECL delay lines

Several MC100EP195 ECL delay lines are used on the iGp12-400F to line up the received RF clock and the fiducial signal. These lines are controlled by registers described in Table 16.

Delay line 0 controls the delay of the ADC clock. Relative delay between lines 1 and 2 is used to achieve reliable detection of the fiducial falling edge in the front-end. Once that relative delay is determined, both 1 and 2 must be adjusted together to achieve proper timing between the fiducial (reset) pulse to the ADC and the ADC clock. This second stage fixes relative delays between 0, 1, and 2. Finally, delay line 3 must be adjusted to achieve optimal placement of the DAC clock relative to the FPGA data.

Table 16: FPGA registers: ECL delay lines

Address	Bits	Definition
0x000130	9:0	Delay line 0 (ADC clock)
0x000131	9:0	Delay line 1 (Fiducial clock)
0x000132	9:0	Delay line 2 (Fiducial)
0x000133	9:0	Delay line 3 (DAC clock)

## 9.6 General-purpose digital I/O

There are two distinctly different drivers implemented in the gateway for the control of the general-purpose digital I/O port of the iGp12-400F. A generic bit-by-bit driver is accessed when bit 16 of the main control register (0x100) is set to 0. The port is accessed via three registers listed in Table 17.

Table 17: FPGA registers: bit-by-bit GPIO

Address	Bits	Definition
0x000138	31:0	Output data
0x000139	31:0	Direction (1 - out, 0 - in)
0x00013a	31:0	Pin value readback

A custom driver designed for interfacing to Dimtel, Inc. longitudinal front/back-end units (FBE) is selected when bit 16 of the main control register is set to 1. The custom driver is included in the gateway starting from version 1.4. Front and back-end phase settings control carrier phases in the front and the back-end respectively. Offset-binary DAC setting in each case provides adjustment range of  $\approx 400$  degrees at the carrier frequency. Front and back-end attenuation settings are in 0.5 dB steps for a total range of 31.5 dB.

## 9.7 Memory

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Table 18: FPGA registers: Front/back-end GPIO

Address	Bits	Definition
0x00013c	11:0	Front-end phase
0x00013d	11:0	Back-end phase
0x00013e	5:0	Front-end attenuation
0x00013f	5:0	Back-end attenuation

## 9.7 Memory

iGp12-400F is configured with two data acquisition memory spaces: block-RAM internal to the FPGA and external SRAM. Memory address mapping is provided in Table 19.

Table 19: Data acquisition memory

Address range	Definition
0x010000-0x01ffff	64k×36 blockRAM (192 ksamples)
0x800000-0xafffff	4M×36 SRAM (12 Msamples)

## 10 Appendix B: Connector Pinouts

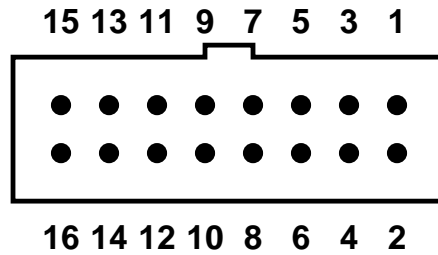


Figure 31: Pin numbering for 16-pin header-type front-panel connectors

Pin numbering scheme for the 16-pin front-panel connectors is shown in Figure 31. Pin definitions for the 8-channel ADC and DAC are provided in Table 20.

Table 20: 8-channel ADC/DAC pinout

Pin number	Definition
1	Channel 7
2	GND
3	Channel 6
4	GND
5	Channel 5
6	GND
7	Channel 4
8	GND
9	Channel 3
10	GND
11	Channel 2
12	GND
13	Channel 1
14	GND
15	Channel 0
16	GND

## Appendix B: Connector Pinouts

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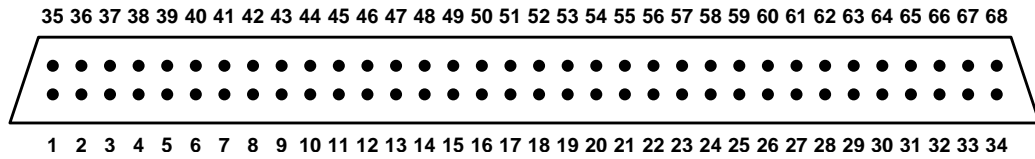


Figure 32: Pin numbering for general-purpose digital I/O connector

Figure 32 shows the pin numbering for the general-purpose digital I/O connector. Pin definitions are listed in Table 21.

Table 21: General-purpose digital I/O pinout

Pin number	Definition
1	Bit 31
2	Bit 30
3	Bit 29
4	Bit 28
5	Bit 27
6	Bit 26
7	Bit 25
8	Bit 24
9	Bit 23
10	Bit 22
11	Bit 21
12	Bit 20
13	Bit 19
14	Bit 18
15	Bit 17
16	Bit 16
17	GND
18	Bit 15
19	Bit 14
20	Bit 13
21	Bit 12
22	Bit 11
23	Bit 10
24	Bit 9
25	Bit 8
26	Bit 7
27	Bit 6
28	Bit 5
29	Bit 4
30	Bit 3
31	Bit 2
32	Bit 1
33	Bit 0
Continued on next page	

**Table 21 – continued from previous page**

Pin number	Definition
34	Bit N/C
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	GND
49	GND
50	GND
51	GND
52	GND
53	GND
54	GND
55	GND
56	GND
57	GND
58	GND
59	GND
60	GND
61	GND
62	GND
63	GND
64	GND
65	GND
66	GND
67	GND
68	N/C





## 11 Glossary

### Glossary

#### **analog-to-digital converter (ADC)**

An electronic circuit that converts continuous analog signals to discrete digital numbers. 5, 6, 10, 14, 16, 17, 24, 31, 44, 46, 49, 51–53, 60, 67, 68, 70–72, 75

#### **blockRAM**

Random access memory integrated in Xilinx<sup>®</sup> FPGA in a form of multiple 18 kbit blocks. 16, 19, 60, 74

#### **Cascaded Integrator Comb (CIC)**

A discrete-time filter, which efficiently averages a large number of input samples. Such filters are typically used for sampling rate changes (decimation and interpolation). 52, 68

#### **digital-to-analog converter (DAC)**

A hardware device to convert a sequence of digital codes to corresponding analog voltages or currents. 4–7, 10, 14, 16, 17, 21, 31, 33, 44, 46, 47, 49, 51, 60, 67, 71, 72, 75, 81

#### **direct current (DC)**

In electrical engineering context — a constant signal, either voltage or current. 68

#### **digital clock manager (DCM)**

A delay-locked loop (DLL) based clock management circuit integrated in the Xilinx<sup>®</sup> FPGA. The circuit allows fine phase adjustment of the output clock relative to the input. 7, 16, 24, 60, 67

#### **delay-locked loop (DLL)**

A device for managing clock skew in digital circuits. 80

**emitter coupled logic (ECL)**

A logic device family in which current is steered through bipolar transistors to compute logical functions. The chief characteristic of ECL is that the transistors are always in the active region and can thus change state very rapidly, allowing ECL circuits to operate at very high speed. 47, 60, 72

**extensible display manager (EDM)**

A tool that manages a collection of active displays with the ability to create and edit display content as well as the ability to execute the same content resulting in the dynamic presentation of live data. 17, 18, 20

**experimental physics and industrial control system (EPICS)**

A set of software tools and applications used to develop distributed soft real-time control systems. 6, 11, 13, 16, 18, 25, 56, 59, 82

**Ethernet**

A family of frame-based computer networking technologies for local area networks. 5, 10

**fast Fourier transform (FFT)**

An efficient algorithm to compute the discrete Fourier transform. 39

**finite impulse response (FIR)**

A discrete-time filter, output of which only depends on a finite number of previous input samples. 4, 7, 21–24, 47, 60, 65–67

**field programmable gate array (FPGA)**

A semiconductor device containing programmable logic components and programmable interconnects. 5, 7, 13, 14, 16, 18, 47, 60, 65, 67, 70–74

**full-scale (FS)**

Difference between maximum and minimum limits of the signal. For example, DAC full-scale is the difference of the outputs for maximum and minimum codes. 6, 10, 60

**input/output (I/O)**

An interface for transferring analog or digital signals to or from the device. 5, 14, 16, 49–51, 53, 73, 75

**input-output controller (IOC)**

An embedded computer used to interface the hardware to the control system. 5, 10, 12–14, 16–18, 39, 43, 45, 56, 58, 59

**Linux**

A Unix-like open-source operating system. 5

**low-voltage transistor-transistor logic (LVTTTL)**

Transistor-transistor logic with the same logic thresholds as transistor-transistor logic (TTL). LVTTTL outputs can be connected directly to TTL inputs. TTL outputs can drive LVTTTL inputs only if the latter are 5 V tolerant. 8, 50, 60

**NIM**

NIM (originally an acronym for Nuclear Instrumentation Methods) logic defines signal levels (with 50  $\Omega$  termination) of 0 V and  $-0.8$  V for logic 0 and 1 respectively. 47

**proportional integral (PI)**

A feedback controller that uses a linear combination of terms proportional to the loop error (difference between the measurement and the setpoint) and to the integral of the loop error. 54

**phase-locked loop (PLL)**

An oscillator, phase locked to the reference clock. Used to synthesize derived frequencies, manage phase shifts and jitter. 24, 31–33

**process variable (PV)**

An individual control or readout signal in EPICS 13, 59

**radio frequency (RF)**

In the accelerator context, a constant frequency constant amplitude signal derived from or phase locked to the storage ring master oscillator. 5–7, 10, 14, 24, 31–33, 36, 56, 58, 60, 67

**root mean square (RMS)**

A statistical measure of the magnitude of a varying quantity. 39, 40, 45

**static random access memory (SRAM)**

A type of semiconductor memory that retains its contents as long as the power is applied. 5, 16, 19, 36, 47, 60, 67, 74

**transistor-transistor logic (TTL)**

A class of digital circuits built from bipolar junction transistors and resistors. TTL defining signal levels:  $V_{OH} = 2.4\text{ V}$ ,  $V_{OL} = 0.4\text{ V}$ ,  $V_{IH} = 2\text{ V}$ , and  $V_{IL} = 0.8\text{ V}$  82

**universal serial bus (USB)**

A serial bus standard to interface a wide variety of devices. 5, 56