LLRF Evaluation Board

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The poster titled "Hypothetical Design for ILC LLRF Hardware" was well received at the LLRF05 workshop in Geneva. While that cartoon of a circuit board is not an appropriate next step to actually build, progress towards that end requires testing of its parts and concepts. This note describes an LLRF evaluation board in the design phase that could prove useful in that regard.

Introduction

This board shares much of its conceptual design with the SNS Interim board, but there are many practical differences, mostly due to four years advancement in calendar time.

	Interim	Production	Evaluation
IF ADC Channels	4 × ADS809	4 × AD6645	4 × LTC22xx
IF DAC Channels	1 (DAC902)	1 (DAC904)	2 (ISL5927)
FPGA	XC2S200	XC2V1500	XC3S1000
Host interface	Ethernet	VXI	USB
Board Size	5.2 × 5.4"	3.8 × 11.9"	3.8 × 5.0"
Board Layers	8	12	6
BGA packages	No	Yes	Yes
Power consumption	8.0 Watts	10 Watts?	5.5 Watts
Input signal	IF	RF	RF or IF
Output signal	IF	RF	RF or IF

Besides the component changes, several new or improved features have been incorporated:

- Sample clock can be derived from LO, with a programmable divider
- Passive resonant IF step-up
- Second high speed DAC channel, could be used for dithering or calibration
- Low latency inter-FPGA communication

The rest of this paper walks through the board design:

- RF/LO Subsystem
- Clocking and Phase Noise
- High Speed ADCs
- Voltage Reference
- Power Supplies
- Miscellaneous Features
- Fabrication
- Status and Conclusions
- Connector Summary
- BOM Summary

RF/LO Subsystem

I considered using a Mini-Circuits LAT-style attenuator at the input to the mixer, instead of three individual 0603 resistors. The LAT-3 is better characterized at high frequencies, but doesn't allow for impedance matching to the mixer. The nod goes to the individual resistors, which are more widely available, and easier to swap using normal tools (like desoldering tweezers).

The mixer used for the downconversion is either a Mini-Circuits SYM-25DMHW or SYM-30DMHW (TTT167 case style). The latter has a 5-3000 MHz range of RF input, covering all accelerator applications under consideration. The IP3 will generate distortion terms on the order of 1% of full scale. This might be adequate for some applications without software correction, and software correction schemes (tied in with phase calibration hardware) could extend linearity to 0.01%.

The power splitter offerings from MiniCircuits are sparse above 2000 MHz. With compatible footprints, the SBTC-2 series two-way splitters and the SCA4 series four-way splitters cover 5 to 2000 MHz.

The following parts can be used to populate the board according to the desired LO and RF frequencies.

U21, U22, U23, U24: 2-way LO splitter

5-1000 MHz	SBTC-2-10
200-2000 MHz	SBTC-2-20
1000-2500 MHz	SBTC-2-25

U13: 4-way LO splitter

5-1000 MHz	SCA4-10
1000-2000 MHz	SCA4-20

M1, M2, M101, M102, M103, M104: level 13 mixer

40-2500 MHz	SYM-25DMHW
5-3000 MHz	SYM-30DMHW

In some applications the downconversion step must be disabled. Examples are initial testing, RF greater than 2000 MHz (with external conversion), and RF less than 100 MHz. In those cases, it should be a simple matter to remove (or not populate) the mixer and input LC network, and jumper from the mixer footprint's RF to IF.

Clocking and Phase Noise

The on-board VCXO/PLL used on previous SNS boards had both advantages and disadvantages. Bench testing of core functionality was simple because the board could free-run. The flexibility for other experiments was limited by the narrow tuning range of the VCXO. Finally, that circuit seems to generate a large part of the system's phase noise.

This evaluation board has no on-board frequency source: external infrastructure must provide a frequency from which the the sampling clock is derived. Keeping the sample clock external makes it practical to use this board in experiments with other accelerating cavities, clock synthesis hardware, and near-IQ sampling strategies, including the 77.761 MHz or 72.222 MHz sample clocks recently proposed for ILC.

The first clock processing chip in the chain is an AD9512. It includes a programmable divider, and can take inputs up to 1.6 GHz, permitting experiments where the ADC clock is derived on-board from the LO. Two outputs go to the DAC chip, and a second clock distribution chip, the ICS83940D. The latter chip has 18 outputs, which seems a little excessive for this board, but it does make sense in the long run. Besides the four ADCs, we need one output for the FPGA clock. I also want at least one output to route to a coax connector for phase noise measurements. So the four-output alternative (ICS8305) isn't enough, and the 18-output ICS83940D fans out enough to use for the cartooned ILC layout that has 14 ADCs on one board. Using it here is good for evaluation purposes.

Evaluating phase noise is an important motivation for building this board. The book values for the clock chain are:

AD9512	0.225	ps
ICS83940D	0.03	ps
LTC2254	0.2	ps
rms sum	0.3	ps

It's clear from reading the data sheets that the ICS parts are pretty good, but ICS doesn't know how to make meaningful phase noise measurements. Test points J24, J25, and J26 are provided for this purpose.

Communicating data from the ADCs to the FPGA means hitting a 5.5 ns long window of valid data out of a 9.5 ns clock period. The only errors that get in the way are the output skew on the ICS83940D and board trace lengths, so this should be easy to hit by setting up every board the same. Communicating data from the FPGA to the DAC, however, requires hitting a much tighter window–perhaps 2.5 ns out of 4.8 ns. The timing errors are also larger, involving output skew of the AD9512 and part-to-part skew of the ICS83940D. Success can be measured by sending a digital test pattern to the DAC, and sweeping the relative clock phase. If the pattern consists of interleaved 0/-1 samples, when the clocks are properly phased a low signal strength should come out. If the bits are received inconsistently across the clock edge, there should be erratic spikes in analog output power.

High Speed ADCs

The LTC22xx series has many attractive features (size, power, price) in theory, but the accelerator community has no experience with it. Parts available in this footprint range from the low-end LTC2225 (12 bits, 10 MS/s) to the high-end LTC2255 (14 bits, 125 MS/s). Table 2 shows a comparison of the 80 MS/s parts in this series with ADCs used in previous generations of SNS boards.

	ADS809	AD6645	LTC2229	LTC2249	
resolution	12	14	12	14	bits
speed	80	105	80	80	MS/s
input 3dB BW	1000	270	575	575	MHz
aperture jitter	0.25	0.10	0.2	0.2	ps rms
latency	5	3.5	6	6	cycles
power	900	1500	246	258	mW
power (idle)	20	N/A	2	2	mW
analog V_{CC}	5.0	5.0	3.3	3.3	V
digital V_{CC}	3.3	3.3	2.0-3.3	2.0-3.3	V
pins	48	48	32	32	
size	9x9	12x12	5x5	5x5	mm
cost	32.44	88.00	22.83	34.58	US$
clock	diff	diff	SE	SE	

A big reason to build this board is to test the LTC22xx ADCs, and in particular the jitter characteristics of its single-ended sample clock on a real multi-converter board.

This board eschews an IF amplifier (and its concomitant power consumption and distortion), and attempts to make do with a step-up transformer. This raises the driving impedance for the ADC input higher than usual. Parasitics in the transformer and ADC can be tuned out, since it only has to operate in a fairly narrow band. More analysis needs to be done regarding the interaction between the IF filter and the ADC switched input circuit.

The longest traces between ADC and FPGA are about 4.5 cm, and the shortest are about 2.0 cm. Assuming a velocity factor $\gamma = 0.65$, the discrepancy introduces a skew of 0.13 ns. That's perfectly tolerable given the minimum design clock period of 9.5 ns. A 50Ω transmission line introduces a capacitance of $C = l/(2Z\gamma^2 c)$, yields 24 pF/ft, or 3.6 pF for our 4.5 cm trace.

The SHDN pins of the LTC22xx ADCs are connected to the same FPGA bank as the other LTC22xx pins. This is the natural way to route the traces, but gives a 2.5 V drive to a 3.3 V input. It should work, since the specified minimum high level is 2.0 V. Changing those banks of the FPGA (and OV_{DD} of the ADCs) to 3.3 V would increase power dissipation and noise, so I won't do that.

Voltage Reference

The temperature coefficients of the on-board references in the high speed ADC (LTC22xx) and DAC (ISL5927) are $\pm 30\,\mathrm{ppm}/^\circ\mathrm{C}$ and $\pm 100\,\mathrm{ppm}/^\circ\mathrm{C}$, respectively. An external reference, the ADR421, will be substituted. The -A suffix part has a $\pm 10\,\mathrm{ppm}/^\circ\mathrm{C}$ stability, $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ broadband noise, and a low 7 Hz $1/f$ noise corner frequency. Starting with the 2.50 V output of an ADR421, resistors are needed to generate the 625 mV reference for the LTC22xx, the 1250 mV reference for the ISL5927, and as well as to provide R_{SET} for the ISL5927. Without resorting to Caddock resistors (huge, $\pm 2\,\mathrm{ppm}/^\circ\mathrm{C}$), the best SMD resistors available from Digi-Key or Newark are made by Susumu; these have $\pm 10\,\mathrm{ppm}/^\circ\mathrm{C}$ coefficients.

When using an external reference, the high speed ADC and DAC chips have temperature coefficients of $\pm 15\,\mathrm{ppm}/^\circ\mathrm{C}$ and $\pm 50\,\mathrm{ppm}/^\circ\mathrm{C}$, respectively. With software temperature correction tables, the input system as a whole will target 20 ppm stability over a 10°C operating range. Board temperature is measured by a DS1822. The mixers will likely be the largest contributor to thermal drift.

To use the LTC22xx ADC chips with their internal references, populate Rx09 instead of Rx08 with zero ohm jumpers. To use the ISL5927 DAC chip with its internal reference, populate R45 instead of R46 with a zero ohm jumper, and remove R35.

Power Supplies

The power budget for board components is as follows:

LTC2254	107 mA	3.0 V	[1], each
ISL5927	83 mA	3.3 V	[2]
CY7C68013A	85 mA	3.3 V	
AD9512	120 mA	3.3 V	
ICS83940D	26 mA	3.3 V	
XC3S1000	12 mA	3.3 V	V_{CCO}, quiescent
XC3S1000	50 mA	2.5 V	V_{CCAUX}, quiescent
XC3S1000	250 mA	1.2 V	V_{CORE}, estimate
ADC to FPGA signalling	88 mA	2.5 V	[1]
FPGA to DAC signalling	116 mA	3.3 V	[2]
Housekeeping	27 mA	3.3 V	

[1] at 105 MS/s; other parts, run slower, dissipate less

[2] at 260 MS/s; less at slower speeds

Assume 5 V pseudo-regulated input, a 90% efficient switcher to generate 1.2 V, and linear regulators for the other voltages. The computed current and dissipation totals are:

draw	voltage	load diss.	total diss.
250 mA	1.2V	300 mW	333 mW
138 mA	2.5V	345 mW	690 mW
428 mA	3.0V	1284 mW	2140 mW
469 mA	3.3V	1548 mW	2345 mW
total		3477 mW	5508 mW

The TPS795xx low-noise regulators have an odd comment in their datasheet: "Although the tab of the SOT223-5 is electrically grounded, it is not intended to carry any current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin." I take them at their word, which requires relying on the thermal conduction through the FR4 circuit board dielectric for heat sinking. I use all four copper layers on either side of the ground planes, interconnected with vias. The area of each thermal pad is approximately 6×8 mm, and the spacing between each layer and ground is 0.13 mm. For a dielectric thermal conductivity of 0.3 W/m/K (I have seen estimates from 0.23 to 0.5), the computed temperature rise for 430 mW dissipation is 1.0 Kelvin. This temperature differential adds to the other temperature differentials in the system, including die to tab and board to ambient.

The voltage regulator footprint is compatible with either the TPS794xx or TPS795xx series (rated at 250 mA and 500 mA, respectively). The latter are not easily obtainable, but this board would require two of the TPS79530 to support highest speed grade ADC, the 125 MS/s LTC2255. All slower ADCs, up to and including the 105 MS/s LTC2254, can be serviced by the TPS794xx. The 2.5V and 3.3V regulators are also used well within the 250 mA limit. For the moment, I choose to put all TPS794xx parts on the BOM, and specify this board only up to 105 MS/s, especially since FPGA programming beyond that speed becomes increasingly difficult.

Jumper slots JT1 through JT8 allow separation of the eight onboard voltage regulators from their loads. For power supply testing, dummy load resistors can be inserted between pins 2 and 3. Final operation will short pins 1 and 2.

Switching power supplies can be problematic to use for low noise data acquisition circuitry like this. The MAX1820Y I chose to run the FPGA core (1.2V) supply is intended for use in cell phones, that have similar noise concerns. Its sync input is attached to the FPGA, so I can plan to put the switching frequency and its harmonics in unobtrusive parts of the IF band. The sync input spec is 15-21 MHz, and the switch frequency is derived by dividing this by 18. So the switching frequency can be firmware tuned from 833 to 1167 kHz. The MAX1820Y has no internal voltage reference; I supply it 0.682 V from a resistor divider driven by the ADR421.

Miscellaneous Features

This board incorporates a total of 12 channels of medium speed baseband analog output, based on 3 AD5624R chips (or their higher resolution siblings). The three chips share clock and frame signals, but have individual data lines, so they can be loaded in parallel. At their maximum clock rate of 50 MHz, all twelve channels can be updated every $0.02 \cdot 24 \cdot 4 = 1.92\mu$s. If the RF sampling clock is in the 80 MHz range, a simple and reliable approach to FPGA programming will use that clock to run the DAC serial data subsystem. This will slow the DAC clock to 40 MHz, and increase the update time to 2.4μs.

A single MCP3208 provides eight 12-bit system analog inputs to the board.

- 0: FPGA core supply current
- 1: LO rms voltage
- 2: Geek port (J7) analog input 1
- 3: Geek port (J7) analog input 2
- 4: Loopback from analog output 2
- 5: Not used
- 6: +5V input voltage monitor
- 7: External attenuator (J20) voltage monitor

Most channels include an RC filter with 20 to 50 μs time constant, to filter out signals faster than can be sampled by the digitizer. The maximum aggregate sample rate of the MCP3208 is 50 kS/s.

There are five LEDs on-board:

- D1: USB present, powered directly from USB connector
- D2: SLED, status of one interconnect line between FPGA and USB interface
- D3: DONE, shows that the FPGA is successfully programmed
- D4: Uncommitted status from FPGA
- D5: Uncommitted status from FPGA

Low latency inter-FPGA communication can be tested with short (150 mm long) 0.5 mm pitch flex cable between two evaluation boards (J3). This is electrically similar to the custom backplane construction proposed for ILC. Termination resistors and voltage banking for 8 differential pairs are set up for LVDS_25 signalling between the FPGAs. The resistor at each transmission end should be removed. One valid setup is to remove R50 through R53 at each end, assigning four pairs for each direction.

The FPGA's HSWAP_EN pin is pulled low, forcing all user I/O pins to a weak-pull-up state at power on. These pins include the ADC SHDN and DAC SLEEP pins, so this system will power on with its high speed ADCs and DAC in low power sleep mode. The AD9512 clock chip also powers up stupid, so after FPGA configuration, the logic needs to use the USB 48 MHz clock to configure the AD9512. I recommend using the FPGA to measure the resulting DSPCLK frequency relative to IFCLK.

The USB 2.0 interface is based on a Cypress CY7C68013A chip, as used on the GNU Radio USRP, the Avnet Virtex-4LX evaluation board, and the LBNL UXO data acquisition board. In combination with a simple FPGA FIFO, it has demonstrated 32 MB/s data transfer to a Linux host. Previous boards used this chip in its 100 pin package, and could dedicate four wires between the USB interface and the FPGA to implement a serial bus for setting registers. This board pushes the design to the (much smaller) 56-pin package, and needs to implement that feature using the JTAG bus.

An SNS-compatible optically isolated interlock connector (J8) is included in the layout, although not listed for population. This is merely a digital input and output for the FPGA; there is no hardwired interlock function like there was on the SNS Interim LLRF board.

Fabrication

This is the first LBNL-designed LLRF board that will include a BGA component. The XC3S1000-4FT256 is small compared to the FPGA used on the Production SNS LLRF board, 256 *vs.* 676 pads.

Ideally, this board will be stacked up from the following layers:

Copper (component side)
2 sheets 1080 prepreg, finished total 0.004853 inches thick
1 oz. copper
0.005 inch core (laminate)
1 oz. copper
4 sheets 2116 prepreg, finished total 0.018213 inches thick
1 oz. copper
0.005 inch core (laminate)
1 oz. copper
2 sheets 1080 prepreg, finished total 0.004853 inches thick
Copper (solder side)

Material names and their thicknesses are adapted from Advanced Circuits web pages. The total thickness is about 38 mils. If the vendor can sneak in more prepreg in the center, to increase the board thickness to about 47 mils, that would benefit mechanical integrity. The 5 mil separation in the outer layers keeps stray inductance down for power pins, and loop antenna area down for signal traces. Line width of 8 mils on FR4 ($\kappa = 4.3$) gives a transmission line impedance of about 50Ω. It's not right to call this a controlled-impedance board, since (with the exception of the LO distribution traces) the longest lines are only $\lambda/50$ long. Advanced Circuits' categorization of this type of custom stack-up is "controlled dielectric." Design rules are 6 mil space, 5 mil trace, 8 mil silkscreen, 12 mil drill, 10 mil annulus. Surface finish should be immersion gold, for compatibility with BGA assembly. This board's 3.8×5.0 inch size should panelize nicely in a 4×4 pattern within an industry standard 16×22 inch sheet, allotting 0.1 inch routing path between boards.

Status and Conclusions

Ideas that will not be tested in this evaluation board, but do need testing somewhere before the suggested ILC design can be considered safe:

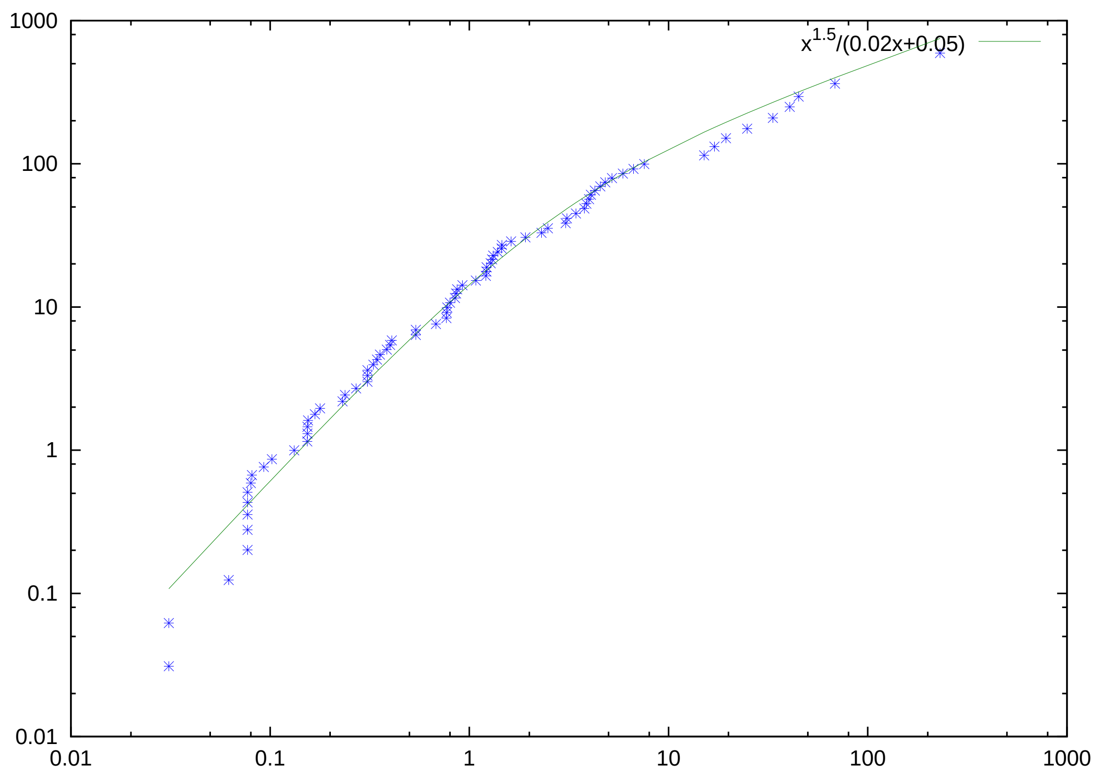
Two-sided ADC layout
FPGA boot ROM with *in-situ* reprogramming
On-board LO amplifier

The four-input-channel configuration is appropriate for studying several applications:

Traditional cavity, forward, reflected, spare
Four-wire BPM
Four-cavity vector sum (or eight cavities, with two boards)

Firmware and software need to be developed for this board. Much of the SNS base still applies, and the core infrastructure for the USB interface has been tested on another project. These two halves will have to be carefully glued together. The board will boot and have its FPGA programmed via USB in three seconds.

At the time of writing, the board layout is nominally complete. Once parts availability is confirmed, and the layout gets reviewed by an assembly house, it can be cleared for fabrication.



Connector Summary

Counterclockwise around the perimeter of the board

J101	SMA	RF/IF input
J201	SMA	RF/IF input
J301	SMA	RF/IF input
J401	SMA	RF/IF input
J15	SMA	LO input (+23 dBm nominal)
J17	SMA	Clock input (+1 dBm nominal)
J7	34-pin header	Geek port (see schematic)
J18	SMA	RF/IF output
J19	SMA	RF/IF output
J20	SMA	Analog output (0 to 2.5V, 2.2 kΩ)
J9	24-pin header	12 channels Analog output (0 to 2.5V)
J8	6-pin Weidmuller	SNS-compatible interlock I/O
J21	LEMO	Trigger
J22	LEMO	Trigger
J6	2.1 mm	+5V, 1.2A pseudo-regulated power input
J1	Type B	USB
J3	20-pin 0.5mm flex	LVDS inter-board communication

RF/IF inputs can be populated either as RF inputs (+10 dBm full scale) or IF inputs (-2 dBm full scale).

RF/IF outputs can be populated either as RF outputs (+1 dBm full scale?) or IF outputs (+7.6 dBm full scale), when used in the first Nyquist zone. No RF filtering is provided, so both sidebands (LO $\pm$ IF) are present.

Interior test points

J23	U.Fl	LO monitor (remove R809 to maintain match)
J24	U.Fl	ICS83940D output 17
J25	U.Fl	ICS83940D output 4
J26	U.Fl	AD9512 output 3
J27	2mm	IF output channel 2
J28	2mm	IF output channel 1
J102	2mm	IF input channel 1
J202	2mm	IF input channel 2
J302	2mm	IF input channel 3
J402	2mm	IF input channel 4

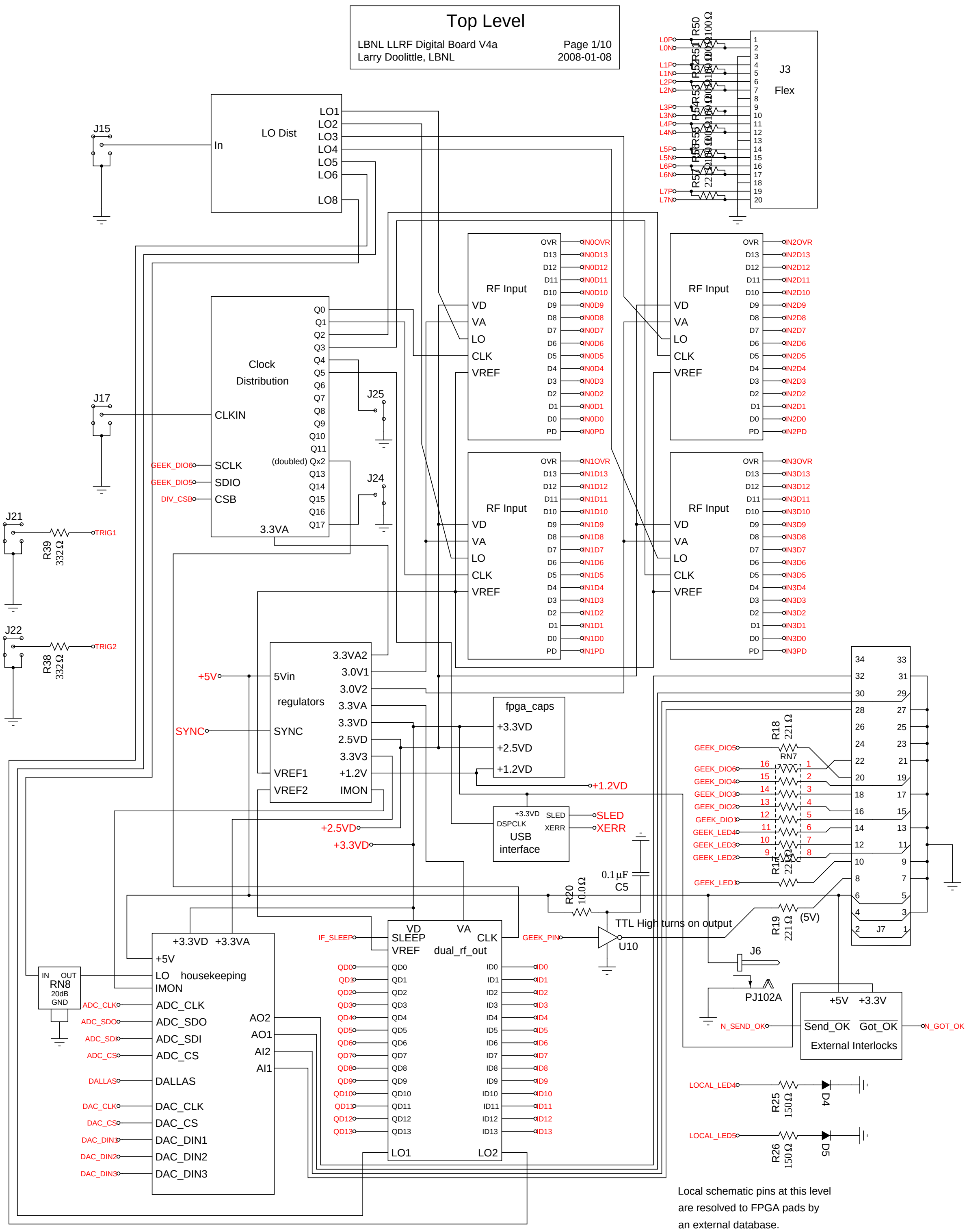
2mm test points are intended for use with a high-impedance single-ended FET scope probe.

BOM Summary

4	QFN32UH	LTC2249	57.6499	230.5996
9	200mil coax compact	ra SMA	7.6100	68.4900
1	QFP-48	ISL5927IN	45.0000	45.0000
1	Xilinx FT256	XC3S1000-FT256	40.5500	40.5500
3	MSOP-10	AD5624R	11.1300	33.3900
2	200mil coax	ra LEMO	12.4000	24.8000
1	LFCSP-48	AD9512	19.4200	19.4200
4	MiniCircuits CD542	ADT16-1T	4.2500	17.0000
1	QFN56LF	CY7C68013A-56LFXC	15.0800	15.0800
1	SO-8	ADR421	7.5500	7.5500
1	LQFP-32 ICS	ICS83940D	6.6700	6.6700
2	MiniCircuits CD542	ADT1-1WT	2.9500	5.9000
4	SOT223-5	TPS79533	1.3000	5.2000
4	hirose ufl	jack	1.2040	4.8160
1	uSOIC-8	AD8361	4.5400	4.5400
69	chip capacitor 0603	0.1 μF	0.0618	4.2642
36	chip capacitor 0805	2.2 μF	0.1133	4.0788
1	SOIC-16	MCP3208	3.9896	3.9896
1	TO-92	DS1822	3.8700	3.8700
2	SOT223-5	TPS79530	1.8900	3.7800
1	header 17x2	user io	3.4300	3.4300
1	uMAX-10	MAX1820YEUB	3.0900	3.0900
5	chip resistor 0603	4.3 kΩ	0.6090	3.0450
1	SOT23-5	INA138	2.4800	2.4800
8	power jump	100mil	0.2876	2.3008
2	chip capacitor 3528	100 μF	0.9570	1.9140
9	octal 0402	100 Ω	0.1800	1.6200
2	chip resistor 0805	2.00 kΩ	0.7280	1.4560
1	hirose fpc 20	FH12A-20S-0.5SH	1.4524	1.4524
1	MiniCircuits DB714	TCM4-19	1.3900	1.3900
4	chip inductor 0603	10 nH	0.3290	1.3160
1	SOT223-5	TPS79525	1.3000	1.3000
16	chip resistor 0603	0 Ω	0.0800	1.2800
1	Panasonic ELL6	4.7 μH	1.2200	1.2200
1	USB type B	AU-Y1007	1.2180	1.2180
1	header 12x2 2mm	generic	1.2100	1.2100
14	chip resistor 0603	681 Ω	0.0770	1.0780
12	chip resistor 0603	150 Ω	0.0770	0.9240
14	chip capacitor 0603	1.0 μF	0.0620	0.8680
1	HC-49/US	24.00MHz	0.8570	0.8570

11	chip resistor 0603	4.75 kΩ	0.0770	0.8470
5	chip diode 1206	Green LED	0.1600	0.8000
1	SO-8	AT24C64A	0.7752	0.7752
10	chip resistor 0603	49.9 Ω	0.0770	0.7700
3	SC-88	MC74VHC1GT04DF	0.2556	0.7668
4	chip inductor 0603	22 nH	0.1700	0.6800
7	chip resistor 0603	100 Ω	0.0770	0.5390
7	chip resistor 0603	221 Ω	0.0770	0.5390
1	chip diode 1206	PMEG2020EH	0.4080	0.4080
5	quad 0603	47 Ω	0.0800	0.4000
5	chip resistor 0603	82.5 kΩ	0.0770	0.3850
4	chip inductor 0603	680 nH	0.0890	0.3560
1	chip resistor 0805	0.47 Ω	0.3440	0.3440
1	CUI-PJ102	2.1mm	0.3300	0.3300
4	chip resistor 0603	2.21 kΩ	0.0770	0.3080
4	chip resistor 0603	10.0 Ω	0.0770	0.3080
4	chip resistor 0603	37.4 Ω	0.0770	0.3080
5	chip capacitor 0603	330 pF	0.0540	0.2700
13	chip capacitor 0603	10 nF	0.0183	0.2379
3	chip resistor 0603	332 Ω	0.0770	0.2310
2	chip inductor 0603	150 nH	0.0890	0.1780
3	ferrite bead 0805	22 nH	0.0560	0.1680
5	chip capacitor 0603	450 pF	0.0310	0.1550
2	chip resistor 0603	124 Ω	0.0770	0.1540
2	chip resistor 0603	84.5 Ω	0.0770	0.1540
8	chip capacitor 0603	1000 pF	0.0192	0.1536
4	chip capacitor 0603	10.0 pF	0.0330	0.1320
3	chip capacitor 0603	47 nF	0.0340	0.1020
3	chip capacitor 0603	100 pF	0.0310	0.0930
1	chip resistor 0603	1.05 kΩ	0.0810	0.0810
1	quad 0603	150 Ω	0.0800	0.0800
1	chip resistor 0603	4.12 kΩ	0.0770	0.0770
1	chip resistor 0603	39.2 kΩ	0.0770	0.0770
1	chip resistor 0603	221 kΩ	0.0770	0.0770
1	chip resistor 0603	68.1 Ω	0.0770	0.0770
1	chip resistor 0603	200 Ω	0.0770	0.0770
2	chip capacitor 0603	12 pF	0.0310	0.0620
1	chip capacitor 0603	220 pF	0.0310	0.0310
1	chip capacitor 0603	47 pF	0.0310	0.0310
6	MiniCircuits TTT167	SYM-25DMHW	DNL	
1	SOIC-8	HCPL-060L	DNL	

1	SOT-23	BCW60DCT	DNL	
10	chip resistor 0603	DNL	DNL	
4	MiniCircuits AT790	SBTC-2	DNL	
6	test point	2mm	DNL	
1	test point	single	DNL	
1	SOT-23	BZX384-C5V6	DNL	
1	MiniCircuits LAT	20dB	DNL	
6	MiniCircuits LAT	2dB	DNL	
12	chip capacitor 0603	0 pF	DNL	
1	SOT-23	MMBD914	DNL	
4	chip inductor 0603	0.3 nH	DNL	
1	weidmuller 2x3	weid6	DNL	
1	MiniCircuits DZ943	SCA-4-10	DNL	
	total			593.9999


Top Level
LBNL LLRF Digital Board V4a
Page 1/10
Larry Doolittle, LBNL
2008-01-08
J3
Flex
LO Dist
In
LO1
LO2
LO3
LO4
LO5
LO6
LO8
J15
Clock
Distribution
CLKIN
SCLK
SDIO
CSB
(doubled) Qx2
3.3VA
J17
J25
J24
J21
R39
332 Ω
TRIG1
J22
R38
332 Ω
TRIG2
GEEK_DIO6
GEEK_DIO5
DIV_CSB
RF Input
VD
VA
LO
CLK
VREF
OVR
PD
regulators
5Vin
SYNC
VREF1
VREF2
3.3VA2
3.0V1
3.0V2
3.3VA
3.3VD
2.5VD
3.3V3
+1.2V
IMON
+5V
fpga_caps
+3.3VD
+2.5VD
+1.2VD
USB
interface
DSPCLK
SLED
XERR
+2.5VD
+3.3VD
housekeeping
+3.3VD +3.3VA
+5V
LO
IMON
ADC_CLK
ADC_SDO
ADC_SDI
ADC_CS
DALLAS
DAC_CLK
DAC_CS
DAC_DIN1
DAC_DIN2
DAC_DIN3
AO2
AO1
AI2
AI1
RN8
20dB
IN OUT
GND
dual_rf_out
SLEEP
VREF
CLK
LO1
LO2
IF_SLEEP
GEEK_PIN
R20
10.0 Ω
0.1 µF
C5
TTL High turns on output
U10
J6
PJ102A
R18
221 Ω
RN7
R19
221 Ω
(5V)
J7
+5V +3.3V
Send_OK
Got_OK
External Interlocks
N_SEND_OK
N_GOT_OK
LOCAL_LED4
R25
150 Ω
D4
LOCAL_LED5
R26
150 Ω
D5
Local schematic pins at this level
are resolved to FPGA pads by
an external database.

RF Input Channel

LBNL LLRF Digital Board V4a — Page 2/10
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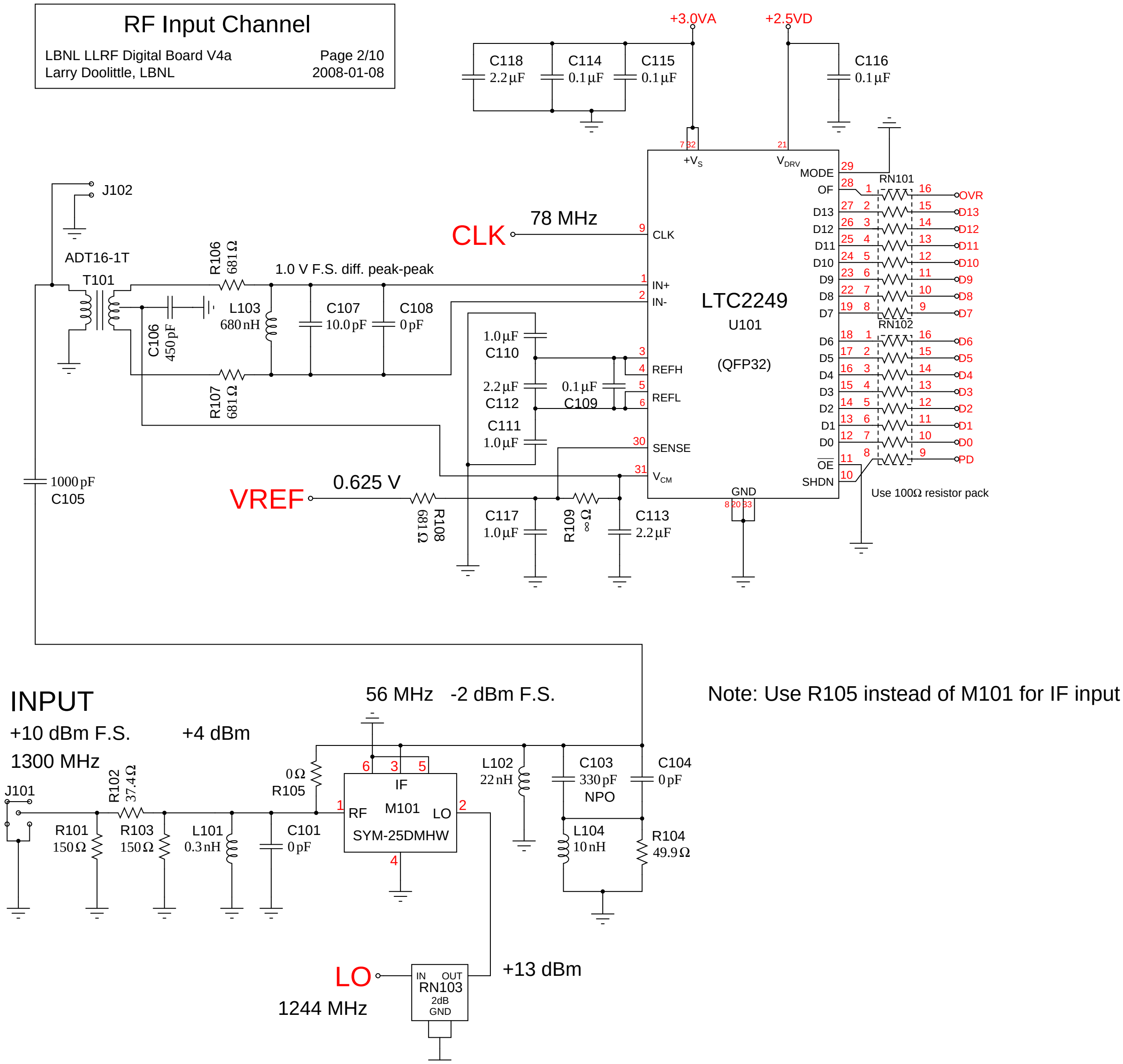

USB Interface

LBNL LLRF Digital Board V4a — Page 3/10

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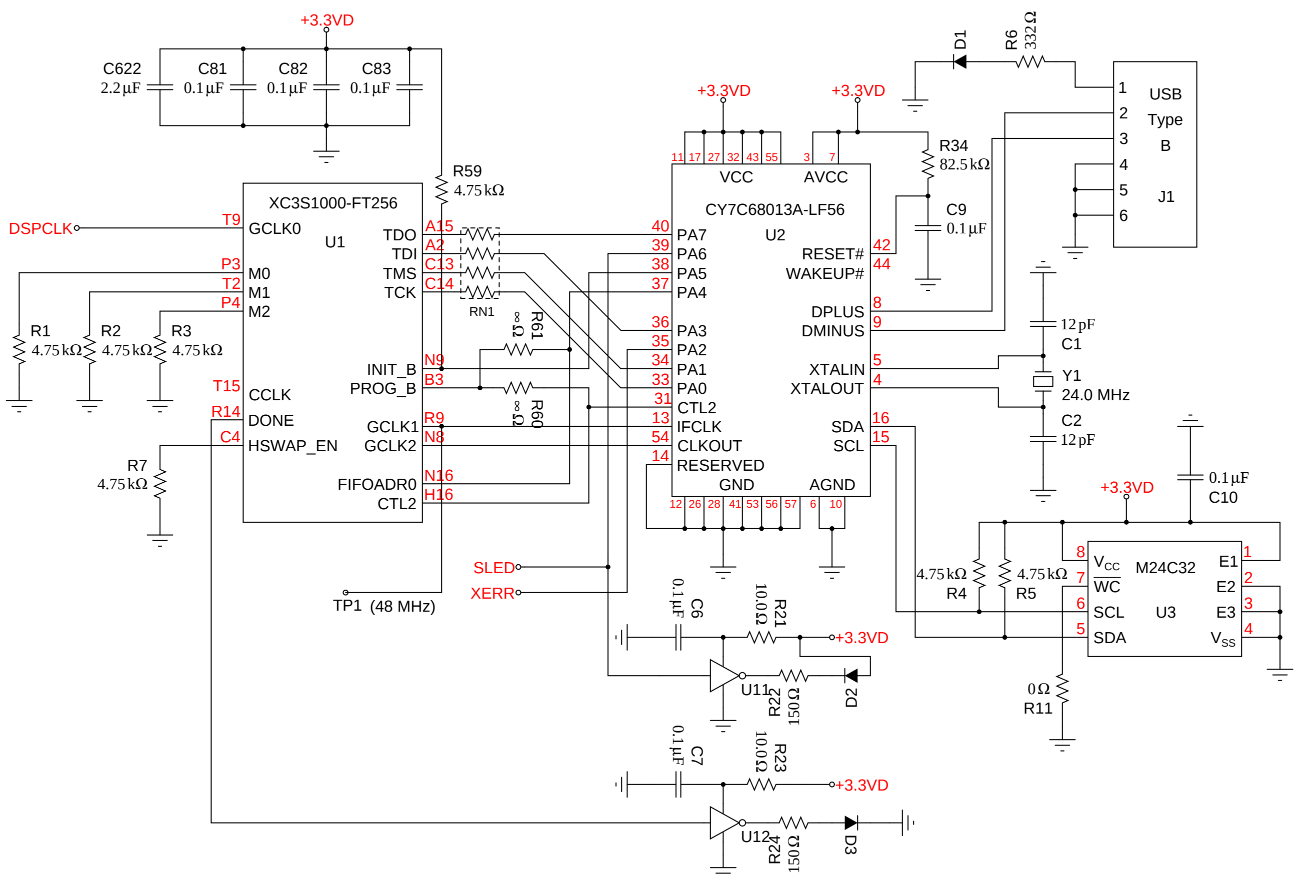

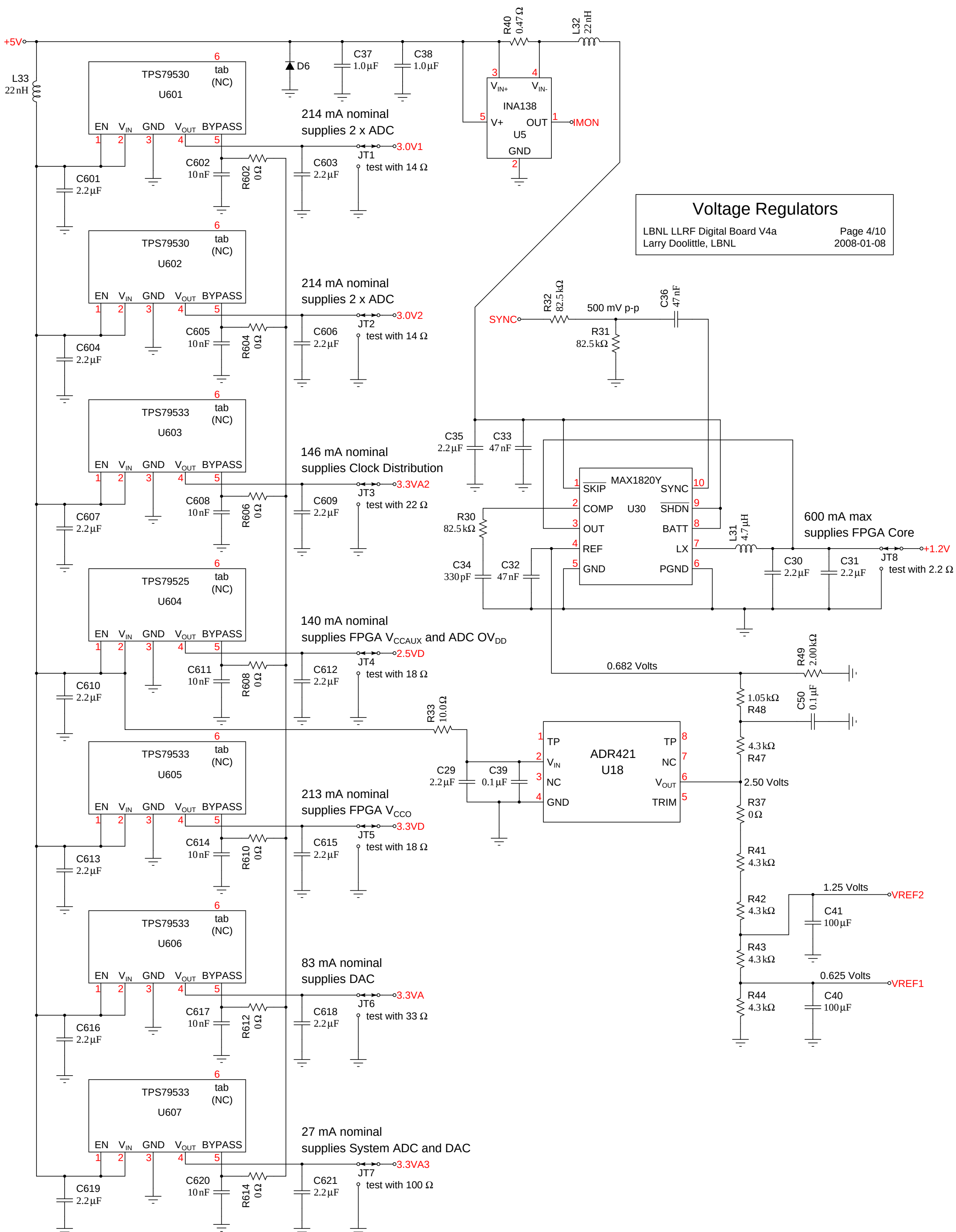
Voltage Regulators
LBNL LLRF Digital Board V4a
Page 4/10
Larry Doolittle, LBNL
2008-01-08
+5V
L33 22 nH
D6
C37 1.0 µF
C38 1.0 µF
R40 0.47 Ω
L32 22 nH
INA138
U5
IMON
TPS79530 U601
214 mA nominal supplies 2 x ADC
3.0V1
JT1 test with 14 Ω
TPS79530 U602
214 mA nominal supplies 2 x ADC
3.0V2
JT2 test with 14 Ω
TPS79533 U603
146 mA nominal supplies Clock Distribution
3.3VA2
JT3 test with 22 Ω
TPS79525 U604
140 mA nominal supplies FPGA VCCAUX and ADC OVDD
2.5VD
JT4 test with 18 Ω
TPS79533 U605
213 mA nominal supplies FPGA VCCO
3.3VD
JT5 test with 18 Ω
TPS79533 U606
83 mA nominal supplies DAC
3.3VA
JT6 test with 33 Ω
TPS79533 U607
27 mA nominal supplies System ADC and DAC
3.3VA3
JT7 test with 100 Ω
SYNC
500 mV p-p
MAX1820Y U30
600 mA max supplies FPGA Core
+1.2V
JT8 test with 2.2 Ω
0.682 Volts
ADR421 U18
2.50 Volts
1.25 Volts
VREF2
0.625 Volts
VREF1

FPGA Power Capacitors

LBNL LLRF Digital Board V4a — Page 5/10
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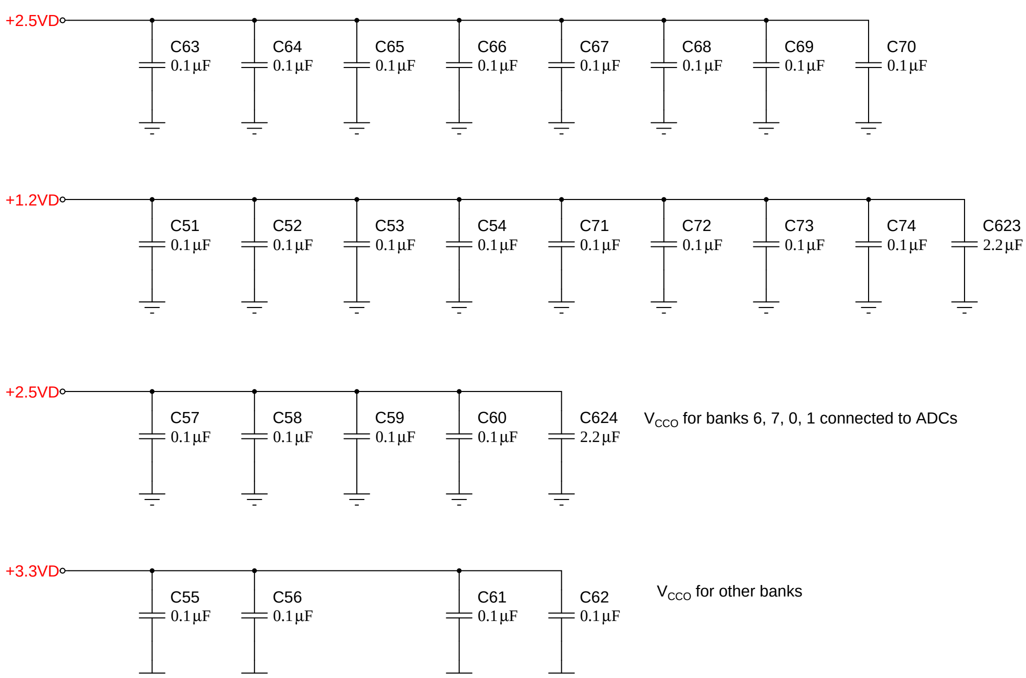

RF Output Channels

LBNL LLRF Digital Board V4a — Page 6/10

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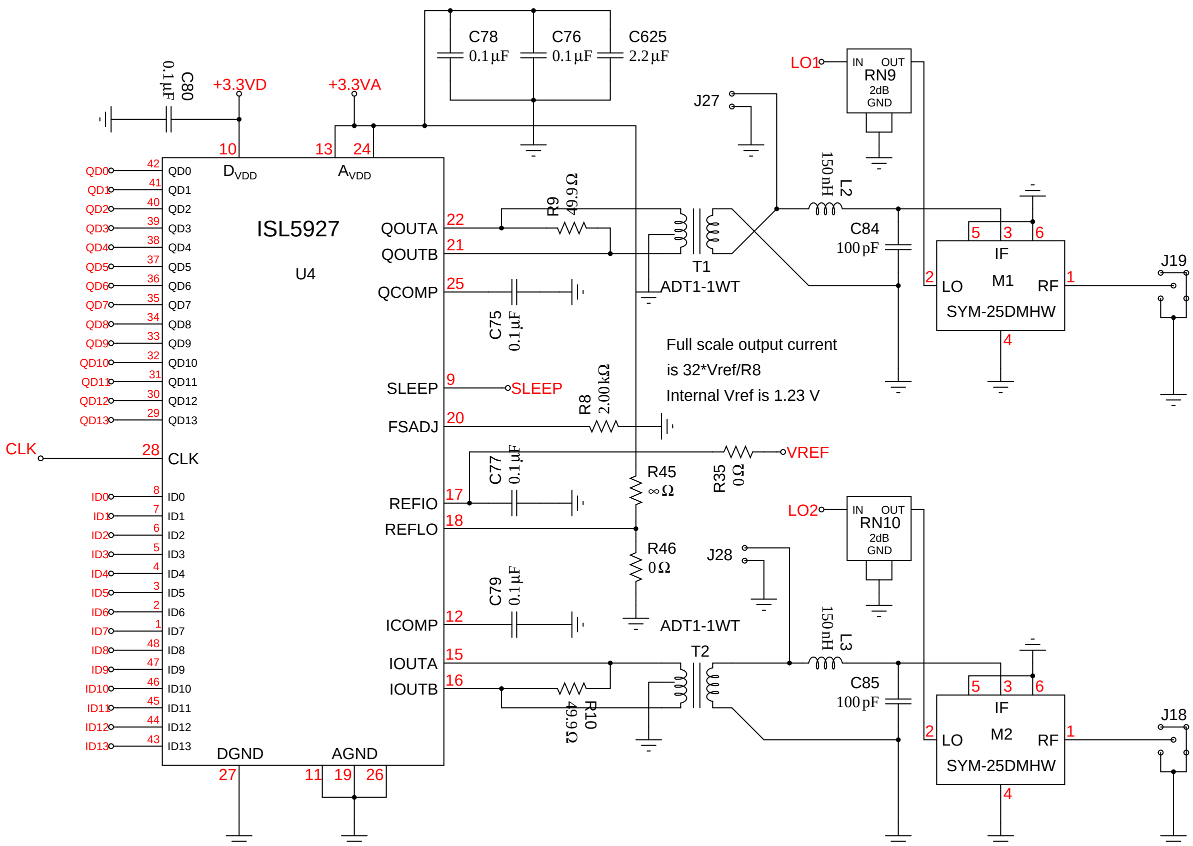
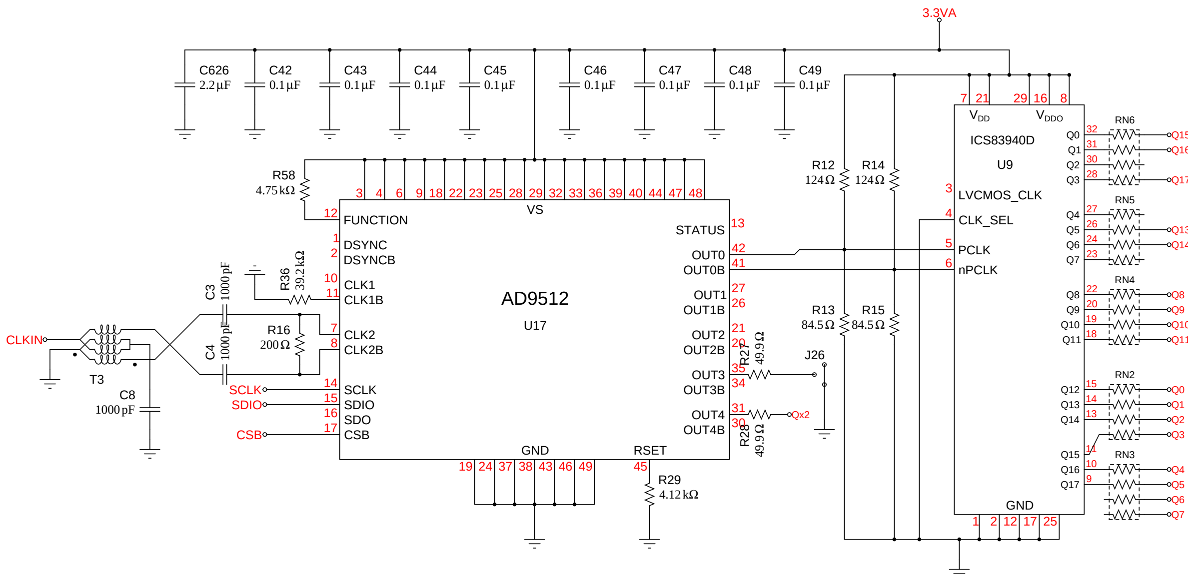


Clock Distribution

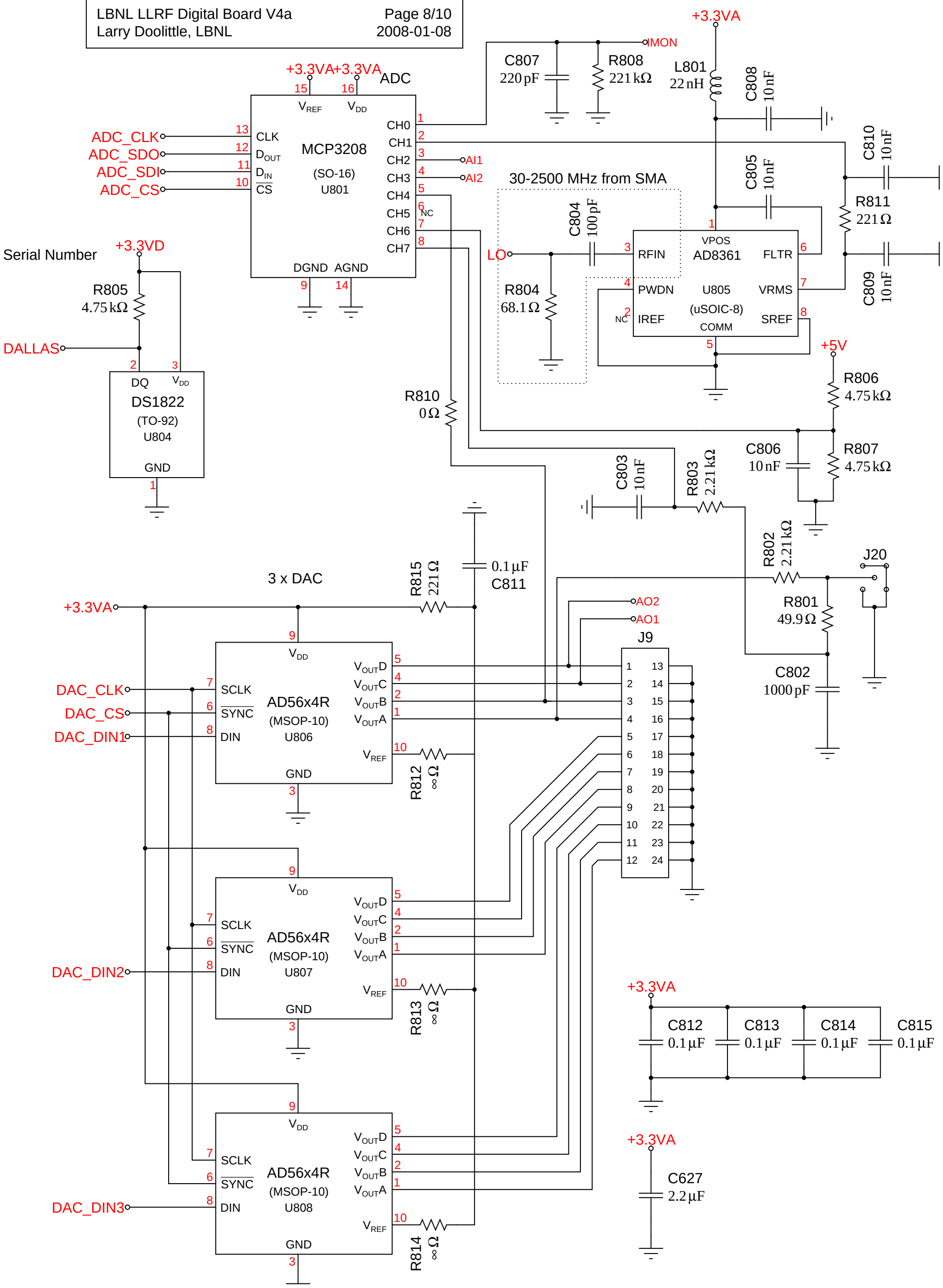
LBNL LLRF Digital Board V4a Page 7/10
Larry Doolittle, LBNL 2008-01-08



Housekeeping

LBNL LLRF Digital Board V4a — Page 8/10

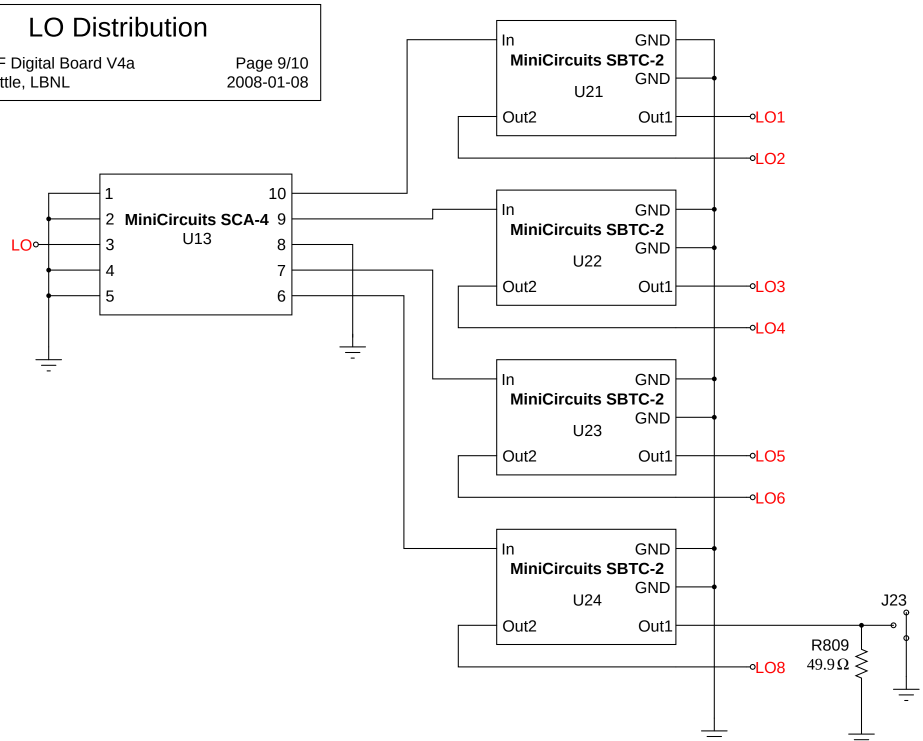
Larry Doolittle, LBNL — 2008-01-08



LO Distribution

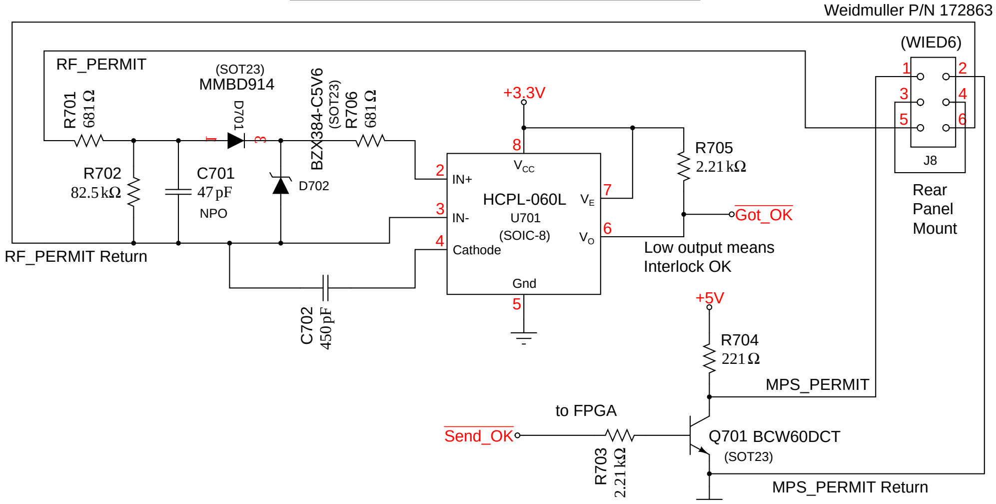
LBNL LLRF Digital Board V4a — Page 9/10

Larry Doolittle, LBNL — 2008-01-08

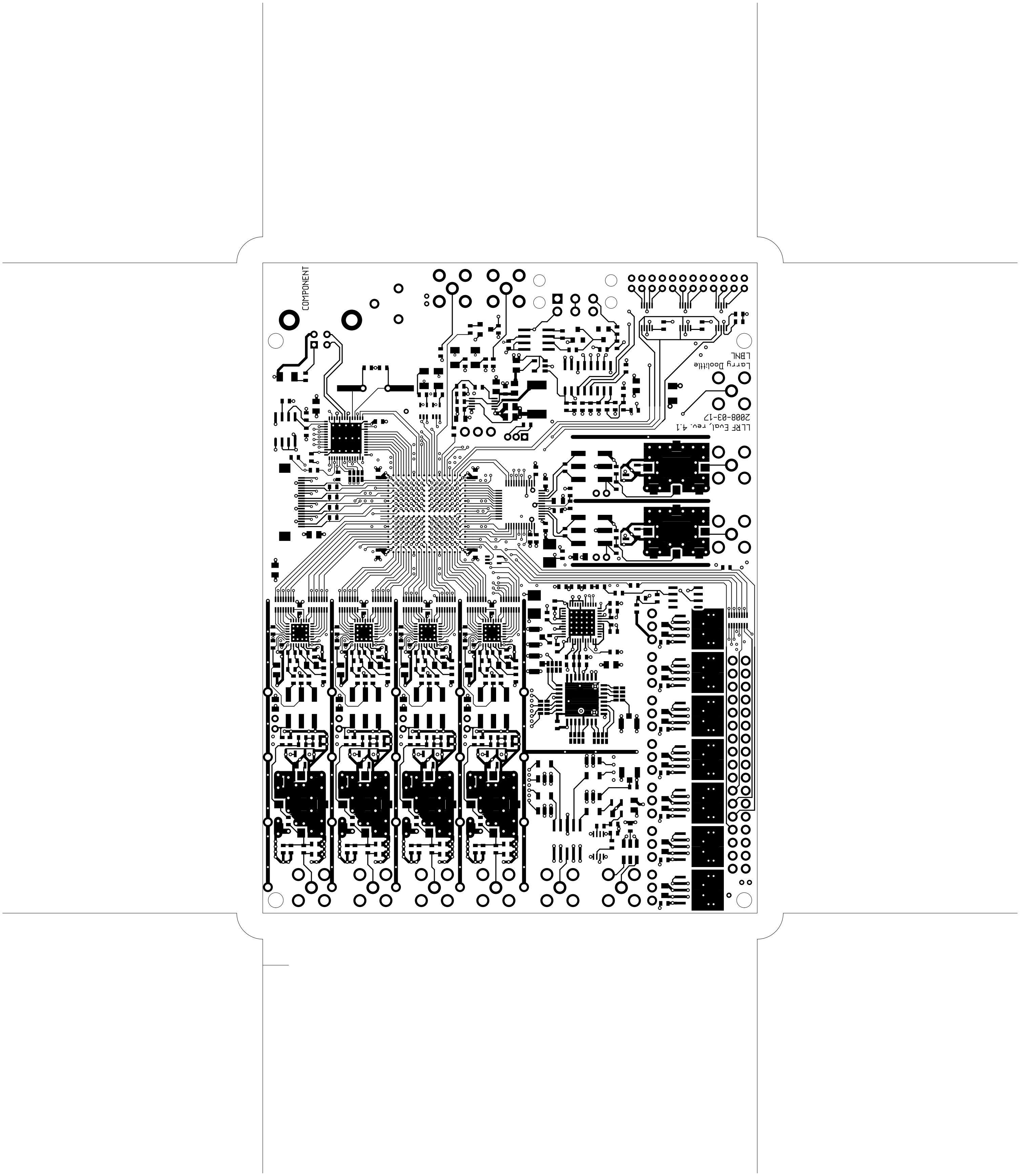


Interlock Input/Output

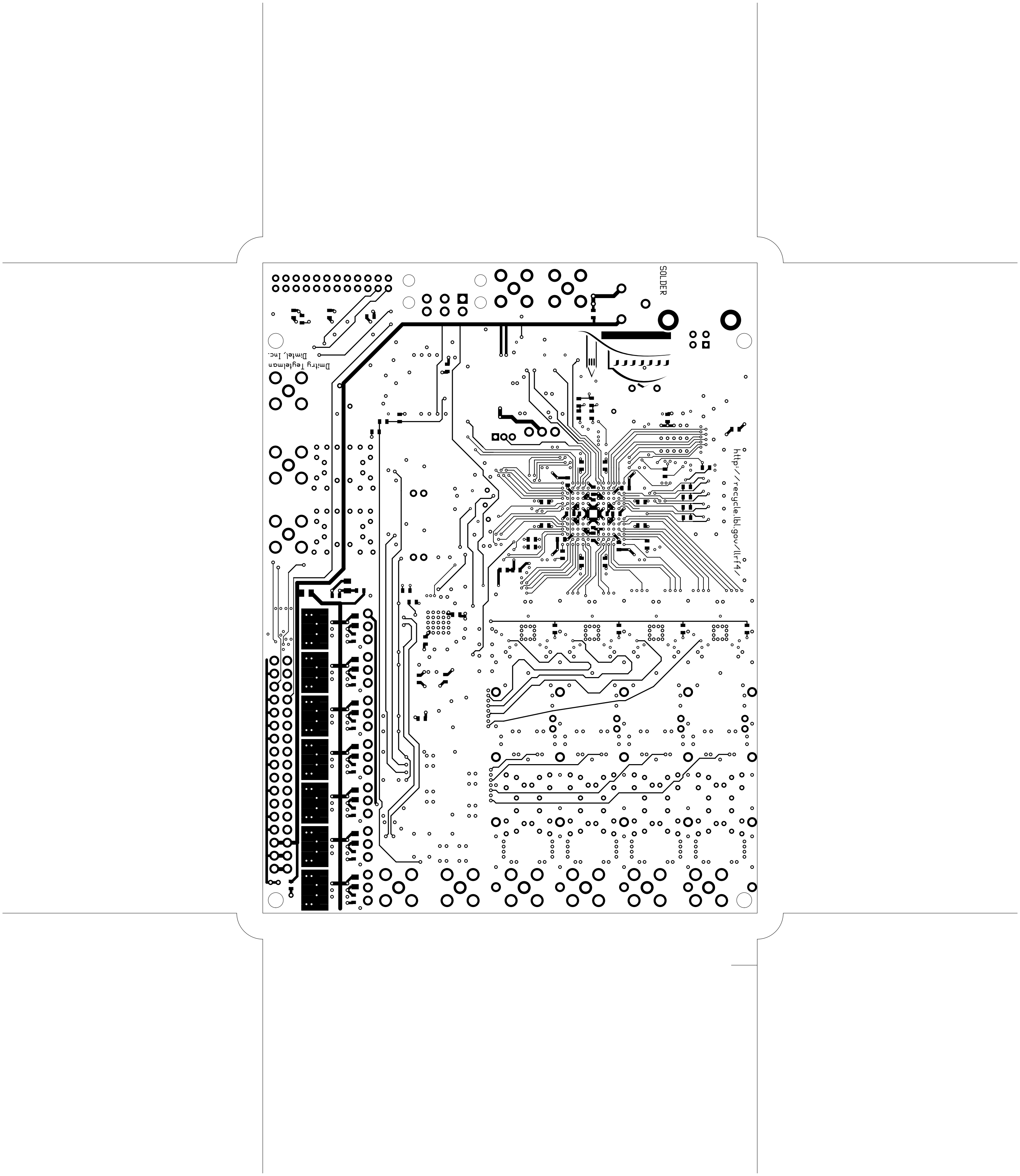
LBNL LLRF Digital Board V4a — Page 10/10
Larry Doolittle, LBNL — 2008-01-08



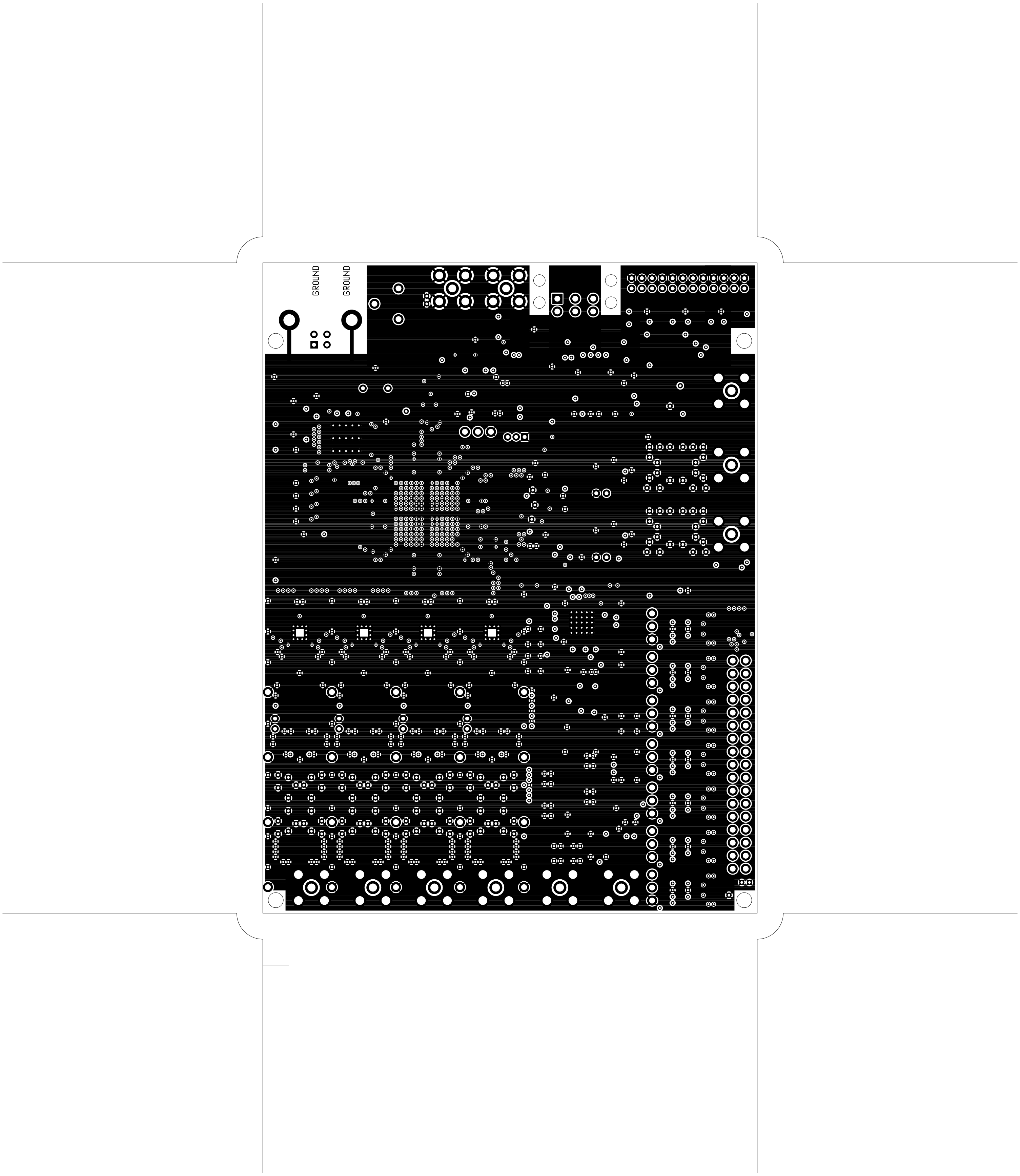
2. component
3. solder
4. GND
5. power
6. signal1
7. componentmask
8. soldermask
9. plated-drill
10. unplated-drill
11. topsilk
12. bottomsilk
13. bottompaste
14. toppaste
15. topassembly
16. bottomassembly
17. fab



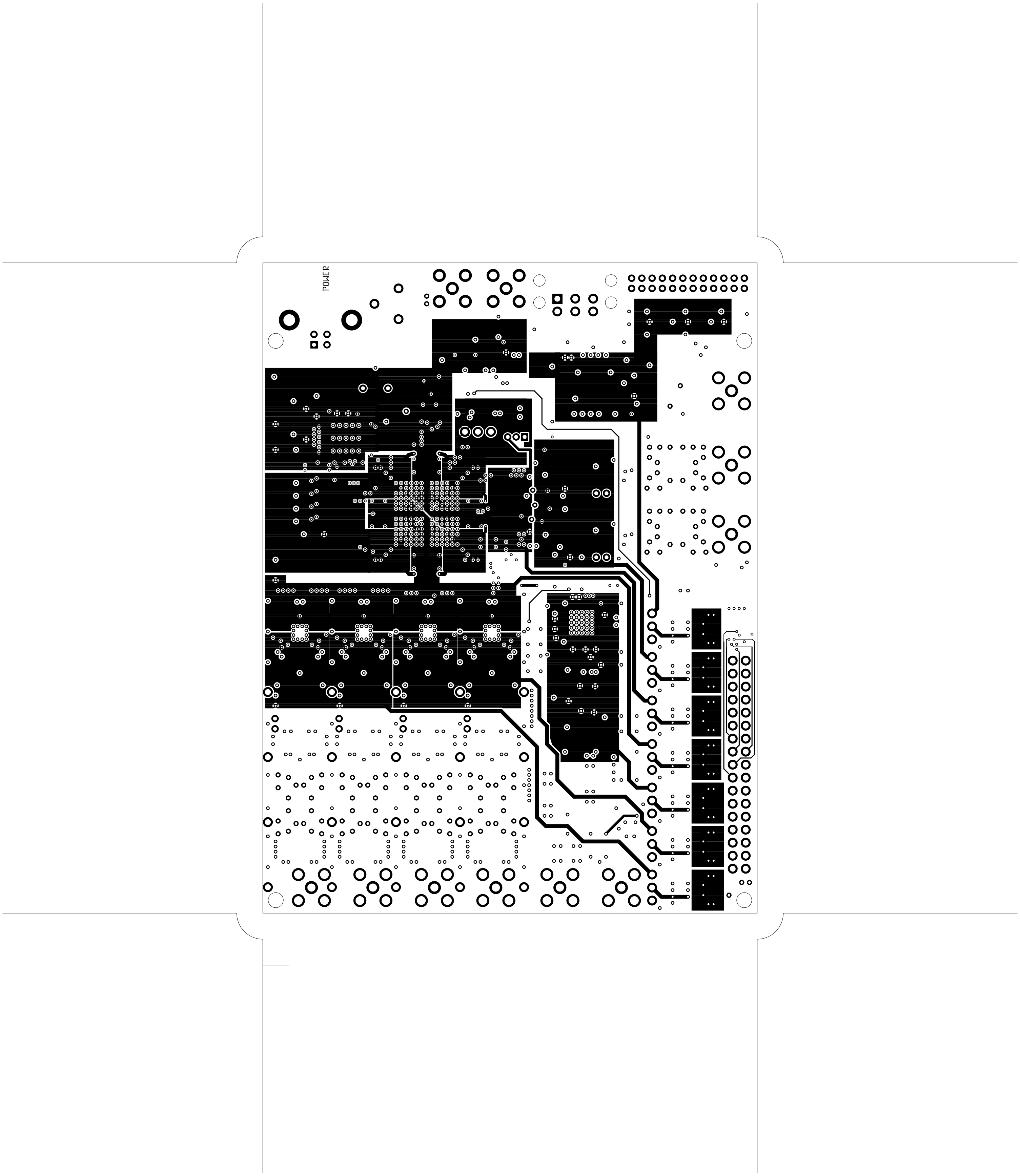
LLRF4, front, scale = 1:1.000
llrf4.pcb



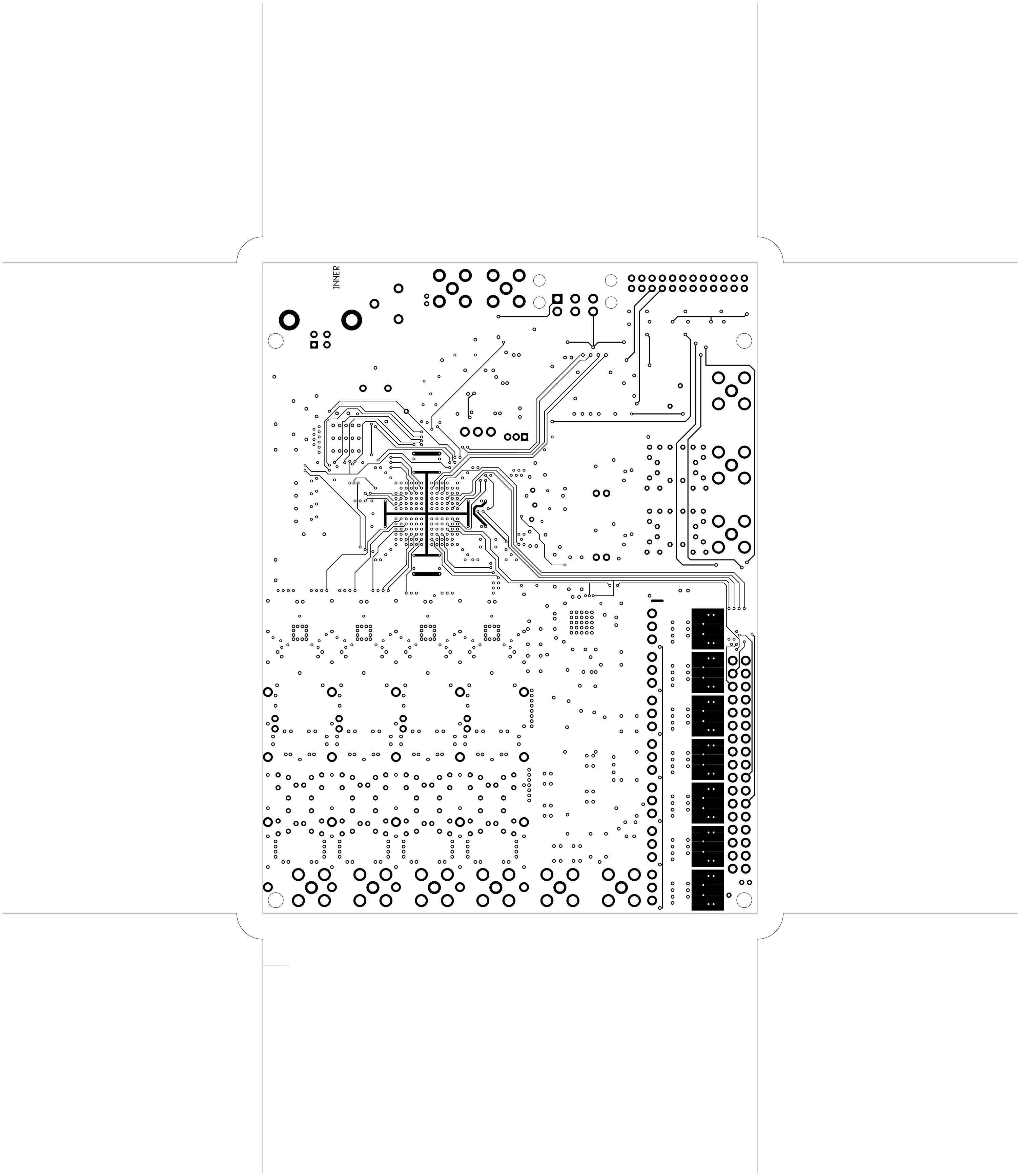
LLRF4, back (mirrored), scale = 1:1.000
llrf4.pcb



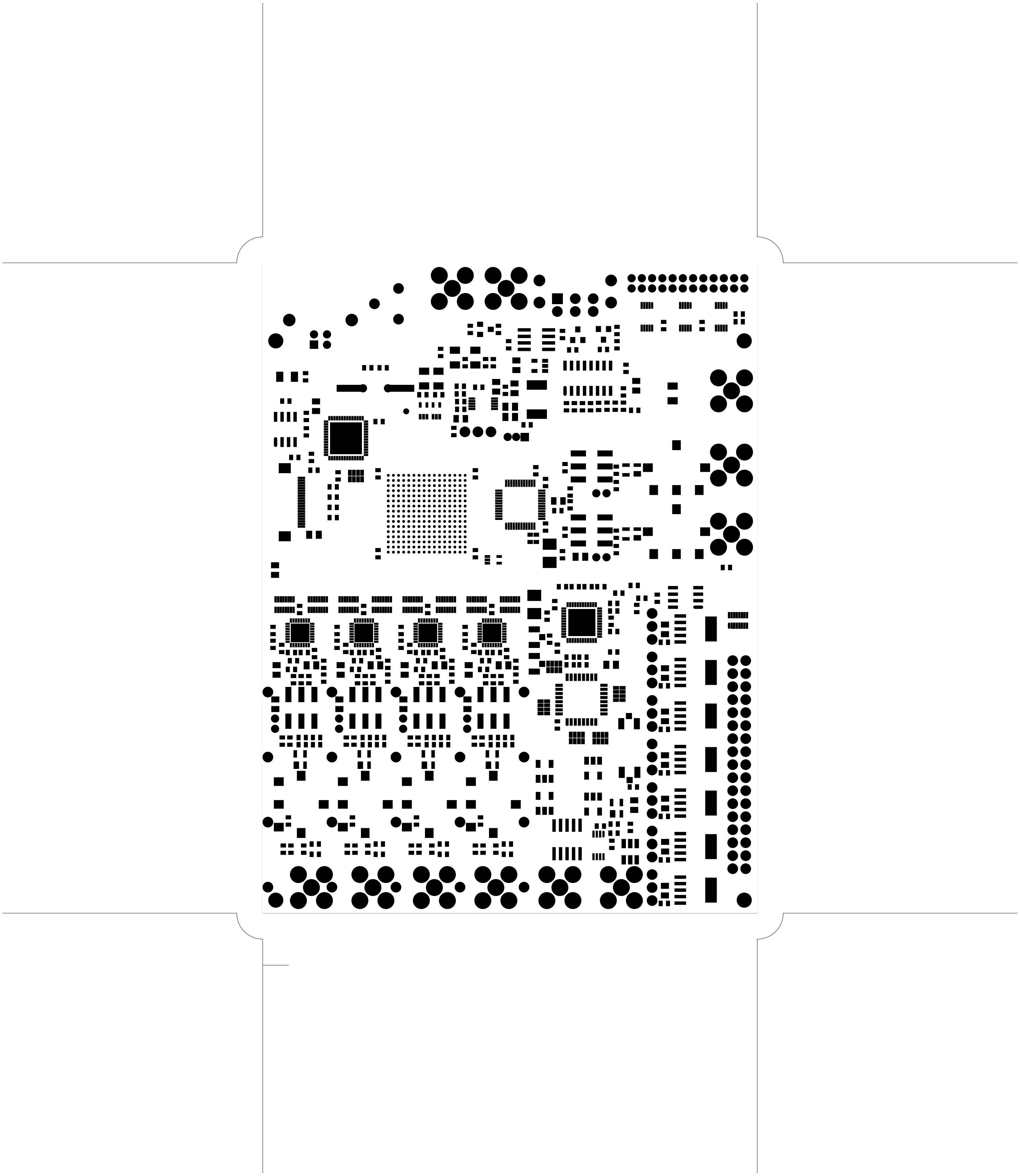
LLRF4, group2, scale = 1:1.000
llrf4.pcb



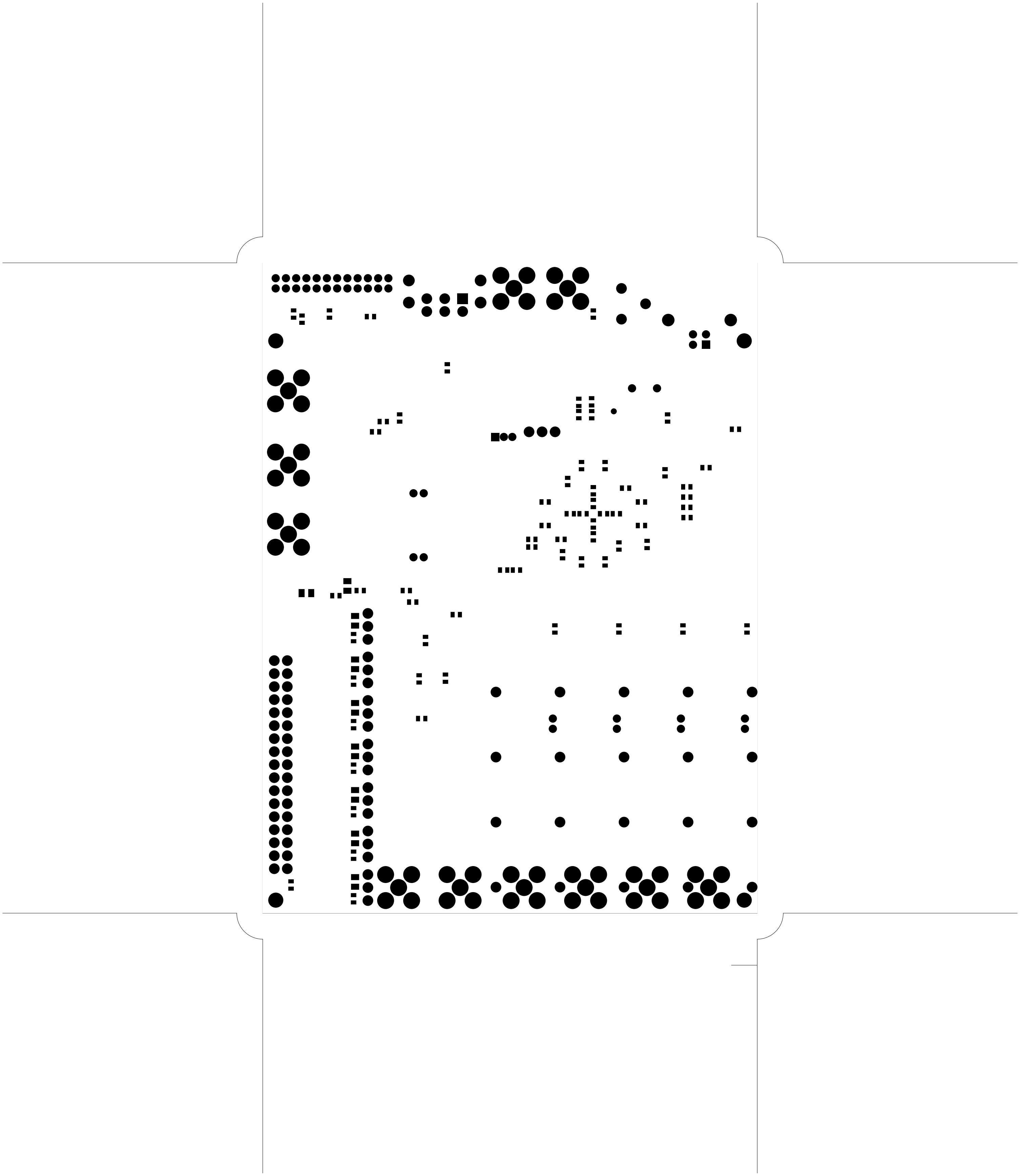
LLRF4, group3, scale = 1:1.000
llrf4.pcb



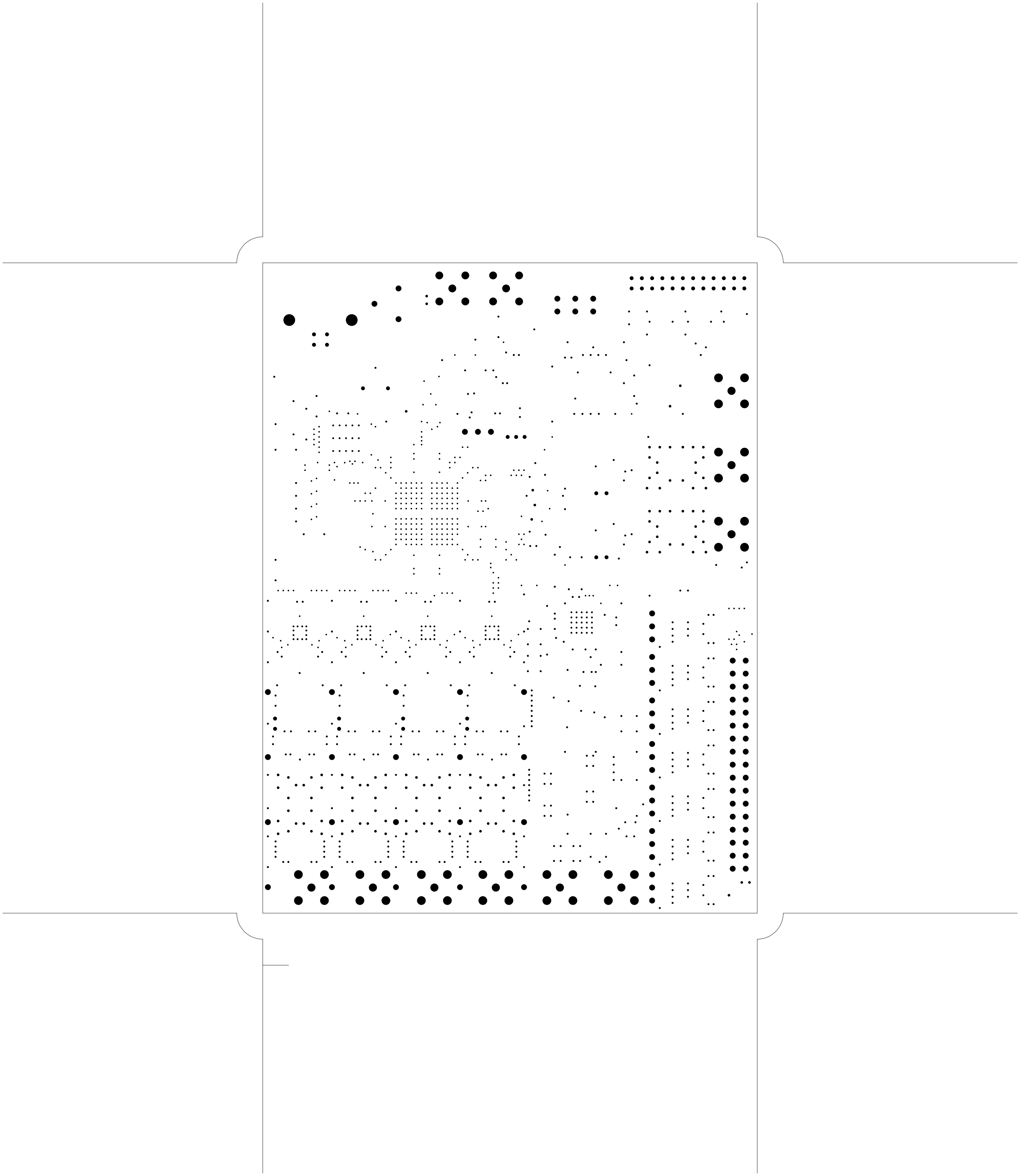
LLRF4, group4, scale = 1:1.000
llrf4.pcb



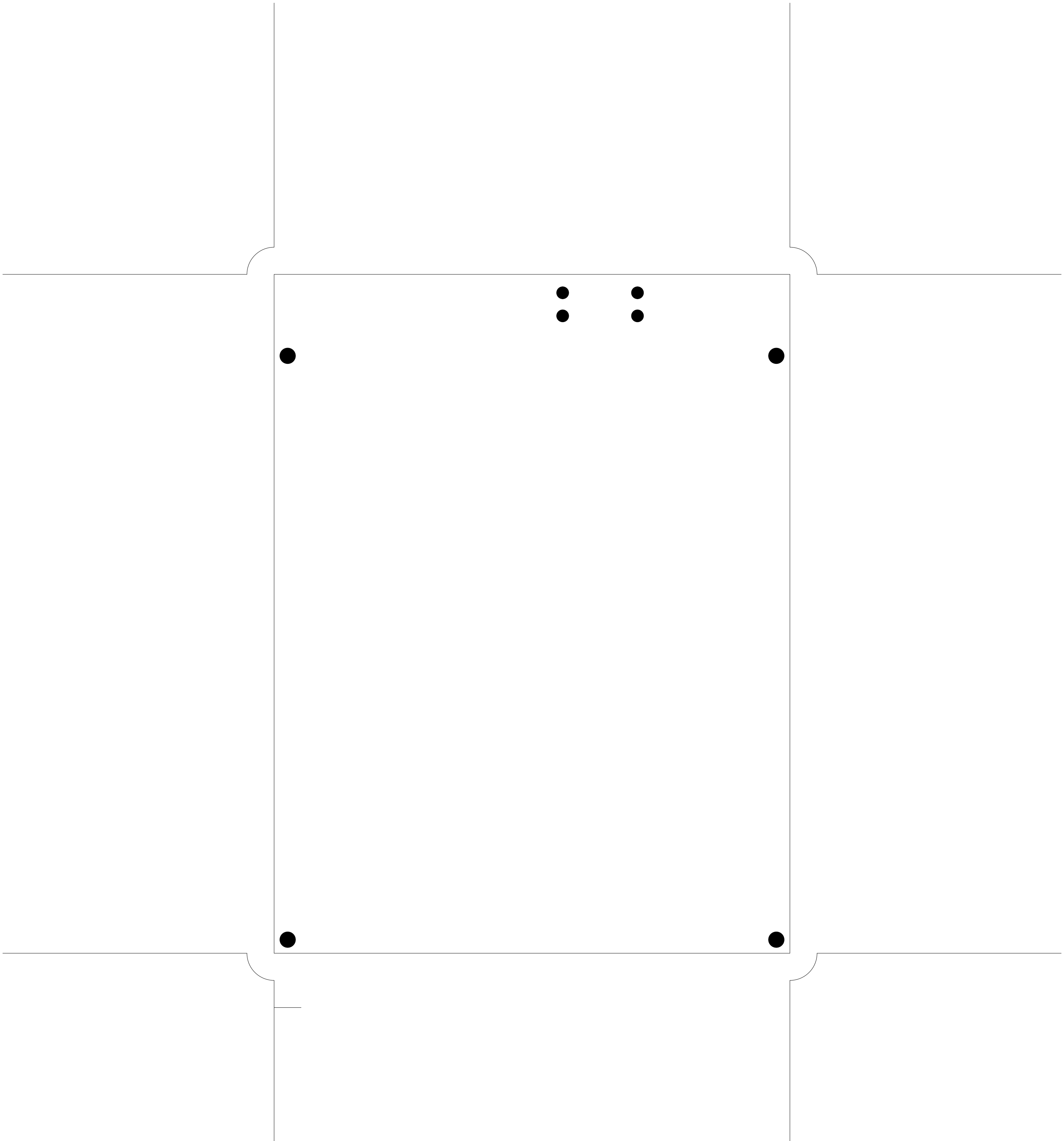
LLRF4, frontmask, scale = 1:1.000
llrf4.pcb



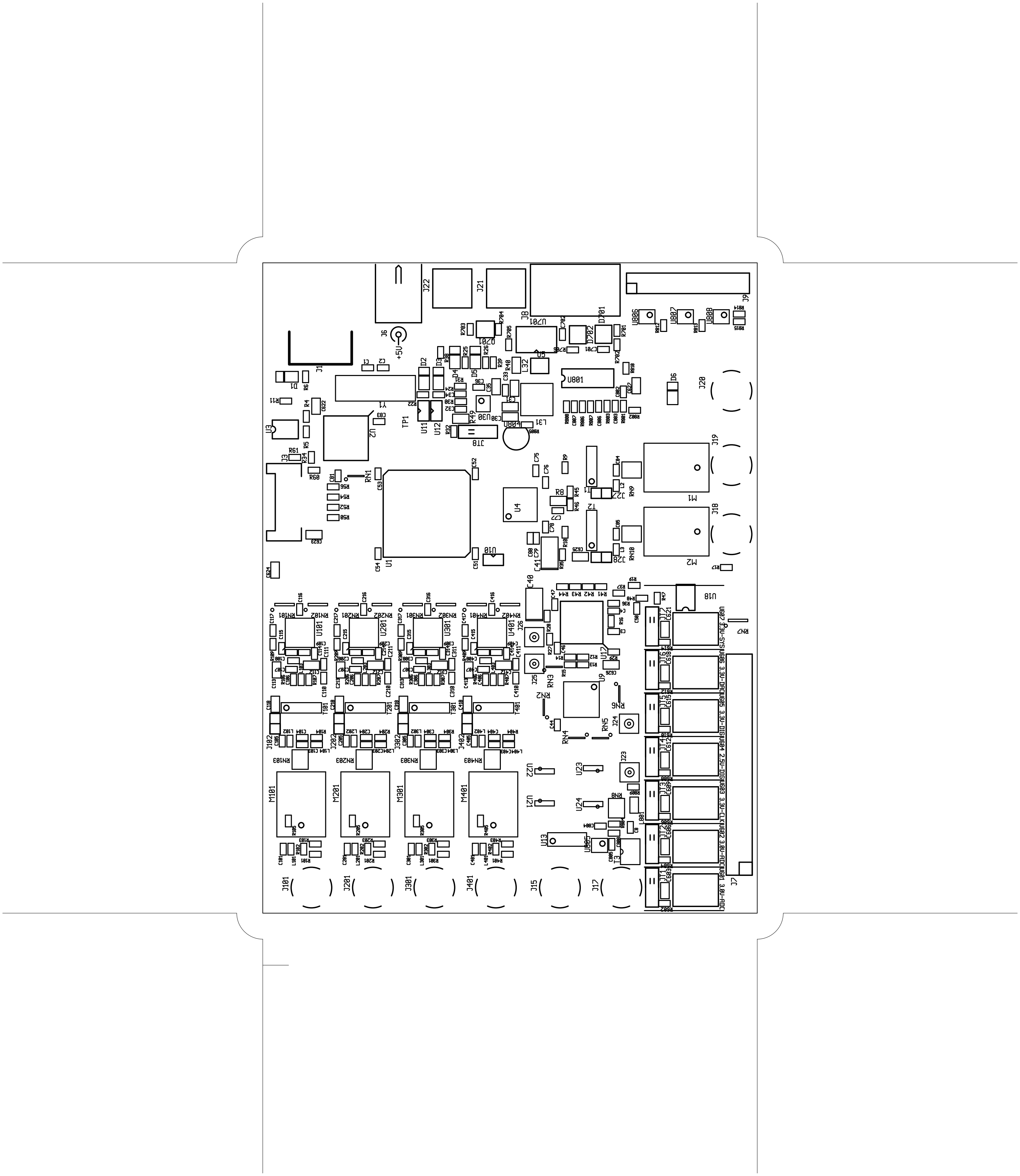
LLRF4, backmask (mirrored), scale = 1:1.000
llrf4.pcb



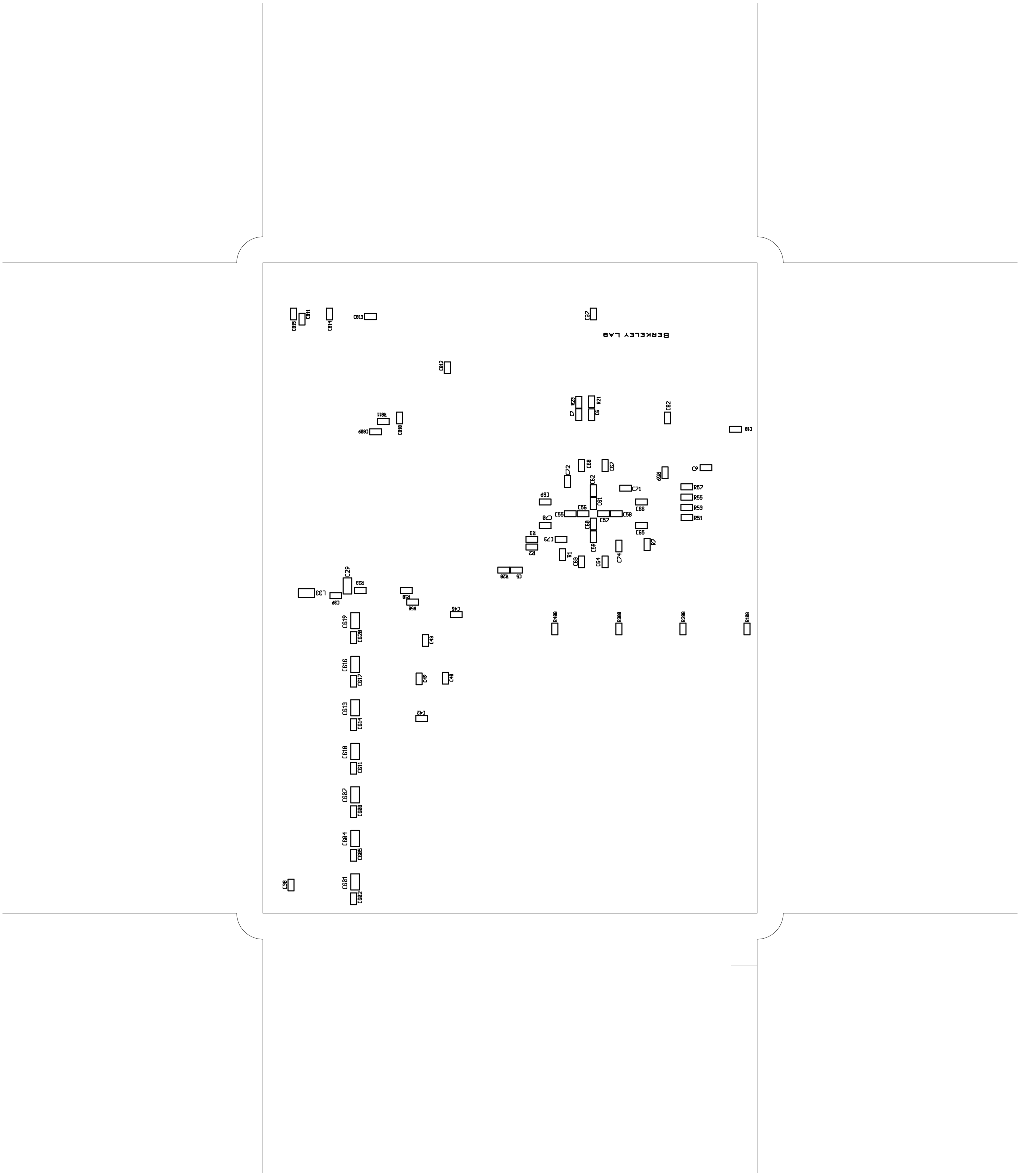
LLRF4, plated-drill, scale = 1:1.000
llrf4.pcb



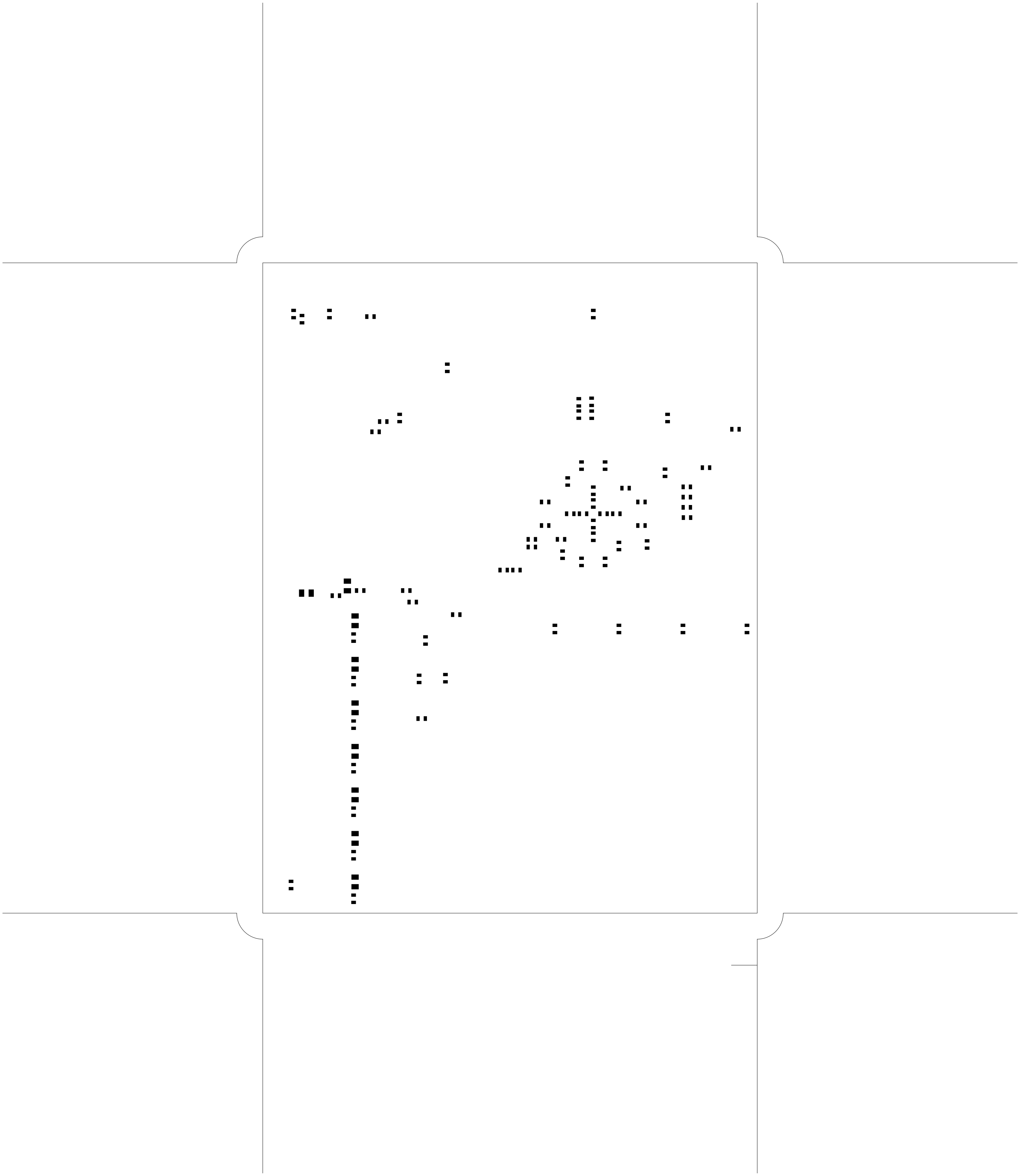
LLRF4, unplated-drill, scale = 1:1.000
llrf4.pcb



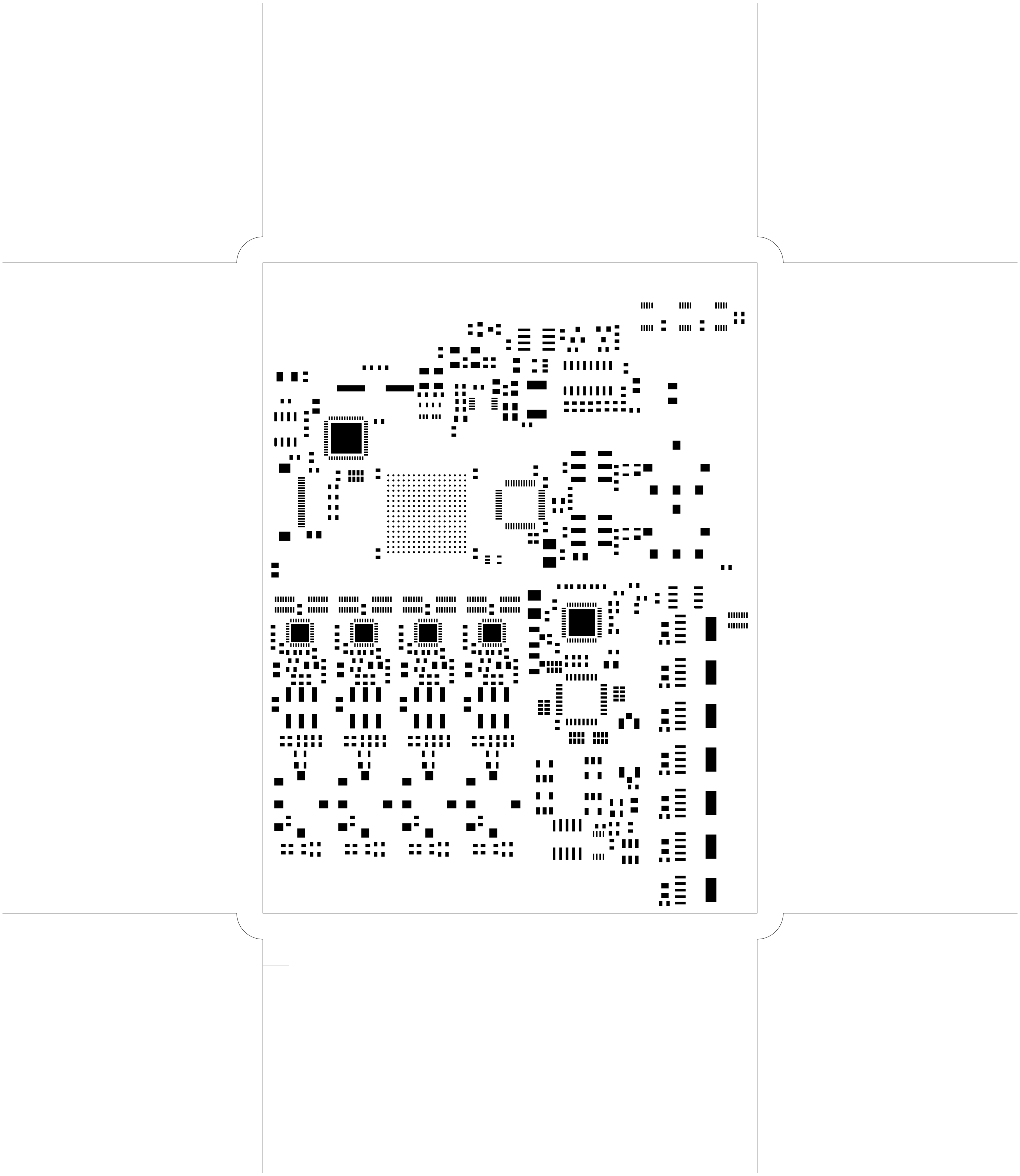
LLRF4, frontsilk, scale = 1:1.000
llrf4.pcb



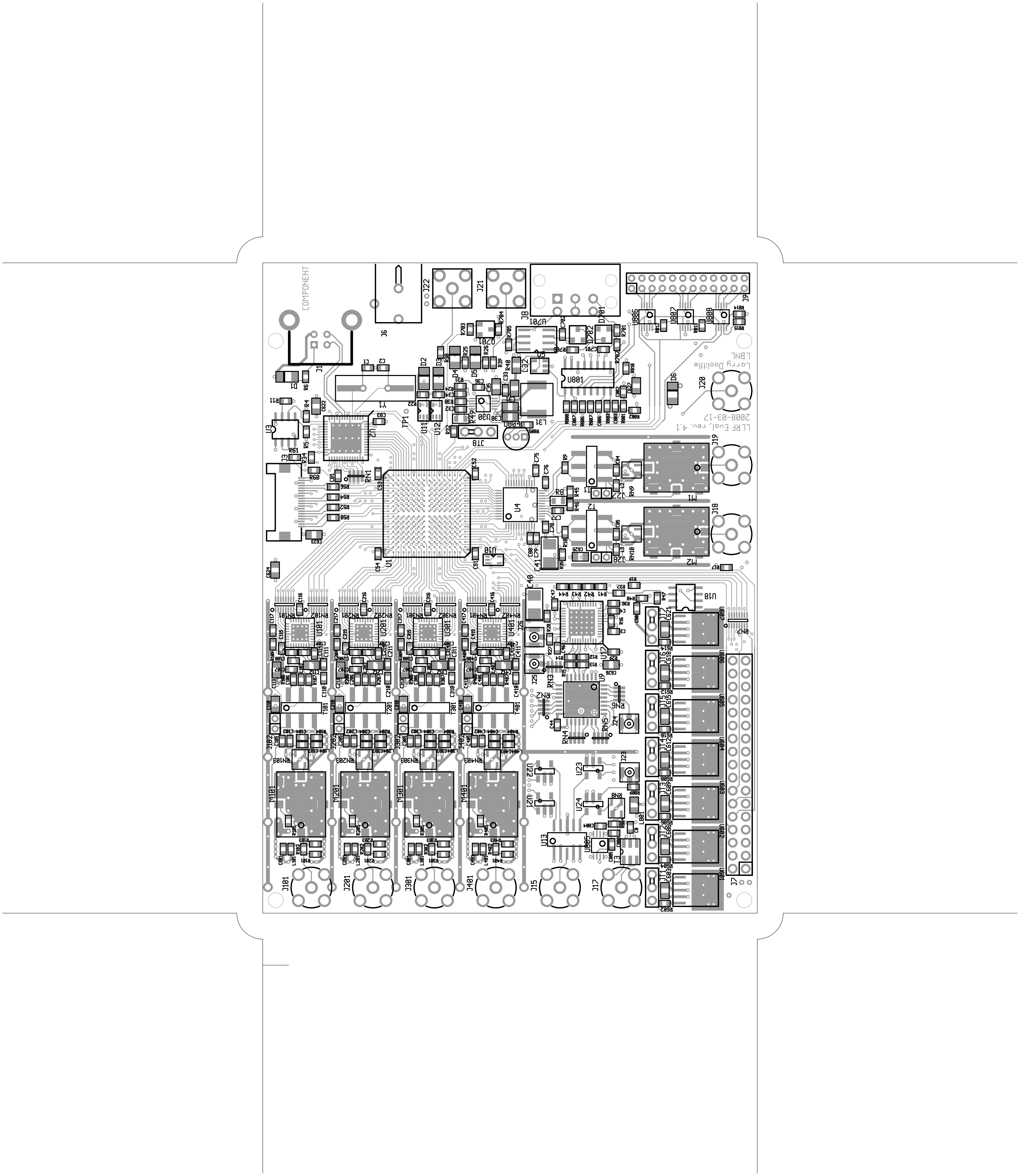
LLRF4, backsilk (mirrored), scale = 1:1.000
llrf4.pcb



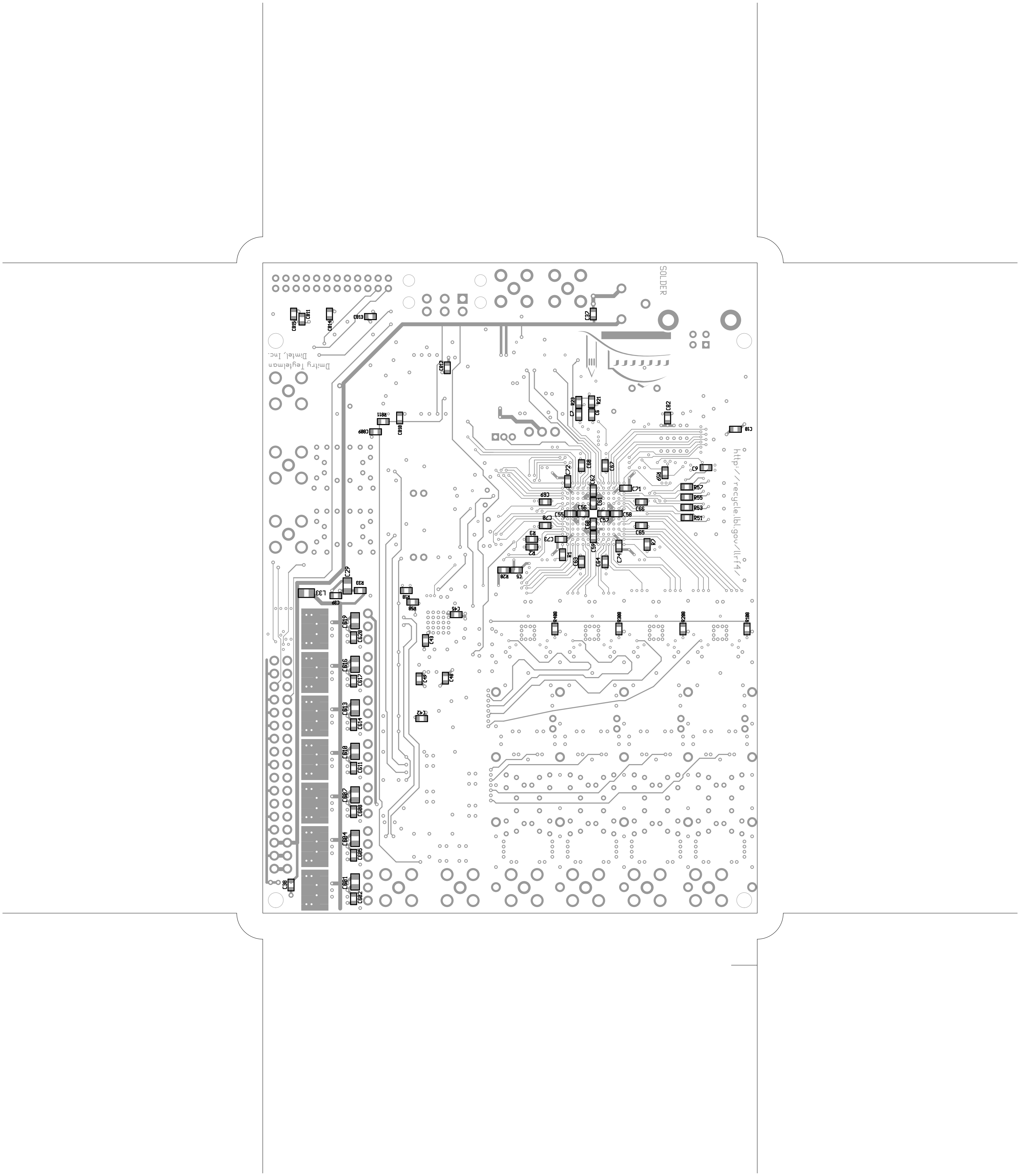
LLRF4, backpaste (mirrored), scale = 1:1.000
llrf4.pcb



LLRF4, frontpaste, scale = 1:1.000
llrf4.pcb



LLRF4, frontassembly, scale = 1:1.000
llrf4.pcb



LLRF4, backassembly (mirrored), scale = 1:1.000
llrf4.pcb

There are 11 different drill sizes used in this layout, 1310 holes total

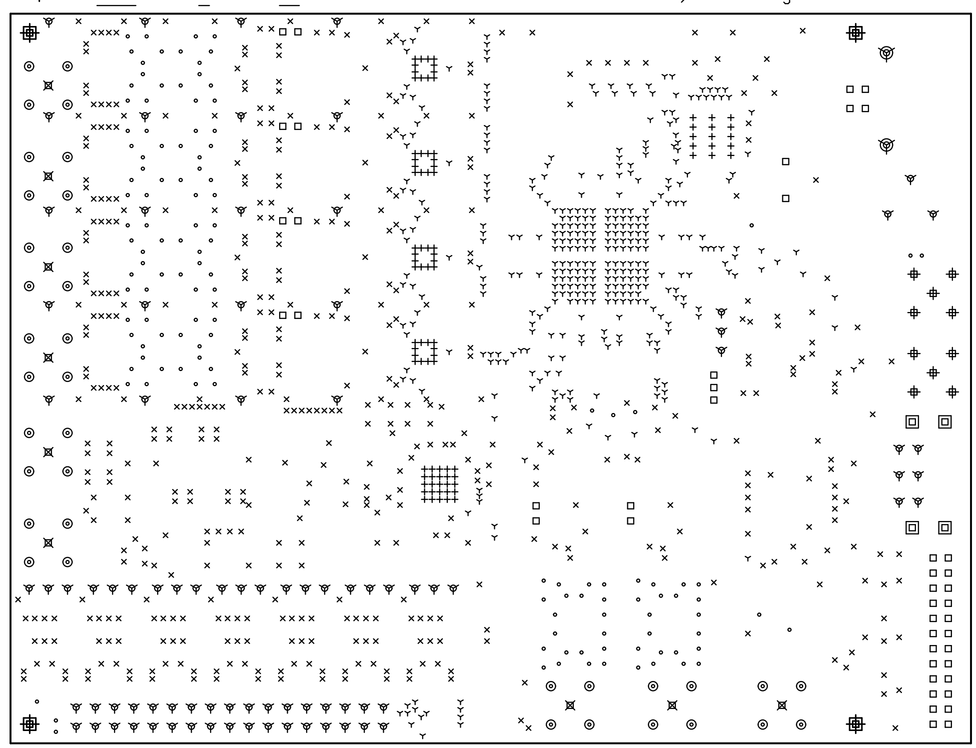
Symbol	Diam. (Inch)	Count	Plated?
	0.012	381	YES
	0.014	88	YES
	0.015	513	YES
	0.020	131	YES
	0.030	45	YES
	0.045	87	YES
	0.060	10	YES
	0.062	9	YES
	0.067	36	YES
	0.090	4	NO
	0.090	2	YES
	0.116	4	NO

Title: LLRF4 - Fabrication Drawing

Author: Dmitry Teytelman

Date: Mon Mar 17 10:53:14 2008 UTC

Maximum Dimensions: 5000 mils wide, 3800 mils high



Board outline is the centerline of this 10 mil rectangle - 0,0 to 5000,3800 mils