iGp12 Factory Test Results

Serial number: iGp12_0067 December 12, 2015

1 Test Procedures and Conditions

1.1 Common settings

All measurements are performed after the unit has been allowed to come to temperature with the ambient temperature of 24 ± 5 °C.

RF clock is set at the nominal frequency, as defined by `IGPF:TEST:RF_FREQ`.

1.2 ADC frequency response

Clock driven by HP8662A at 0 dBm level. `ADC+` input is driven by HP8664A at -8 dBm. Set data acquisition length to 0.4 ms. Response is measured at 53 points between 10 MHz and 1.99 GHz as follows:

```
[amp,fr,RMS] = adc_fsweep_fast('TEST',linspace(10e6,1990e6,53));
```

Matlab figure window 2 is printed to `adc_fsweep.eps` and 3 dB bandwidth is recorded in `measurements.log`.

1.3 ADC performance

Clock driven by HP8664A at 0 dBm level. `ADC+` input is connected to HP8662A via two Mini-Circuits SLP-21.4 filters in series. HP8662A is set to 2 dBm output level. Signal frequency is computed as

$$f_{\text{in}} = \lfloor \frac{20 \times 10^6}{f_{\text{bin}}} + 0.5 \rfloor f_{\text{bin}} \quad (1)$$

$$f_{\text{bin}} = \frac{f_{\text{clk}}}{N} \quad (2)$$

where N is the acquisition length (`IGPF:TEST:RECLEN`). Data acquisition length set to 0.4 ms. ADC characterization is performed by the following function:

```
[sol,RMS,D,amp,f,x,x_fit,SNR,SINAD,SFDR] = adctest('TEST',10);
```

Matlab figure window 2 is printed to `SFDR.eps` and window 3 — to `adctest.eps`. Record average SFDR and SINAD, compute effective number of bits as `(mean(SINAD)-1.76)/6.02`.

Measure ADC signal level using HP4396A in the spectrum analyzer mode, then compute full-scale level by adding `20*log10(2047.5/mean(amp))`.

1.4 ADC step response

Signal source is SRS CG635 with `Q HIGH` set to 0.5 V and `Q LOW` to −0.5 V. Generator output is connected to the iGp12 via a 5 dB attenuator. Unused output of CG635 is terminated into 50 Ω. Set CG635 to 36.001 MHz, data acquisition 0.4 ms and measure the step response:

```
[delay,val,x] = step_response('TEST',36.001e6);
```

Print Matlab figure window 1 to `adc_tsweep.eps`. Record rise and fall times, overshoot and undershoot in `measurements.log`.

1.5 Transfer function measurements

Calibrate HP4396A in the network analyzer mode (using Mini-Circuits ZFSC-2-11-S+ splitter) for S_{21} measurements from 10 MHz to $0.98 \times f_{\mathrm{clk}}$. Perform 4 transfer function measurements:

1.5.1 Feedthrough

DAC output turned off, measurement of the feedthrough. Averaging factor of 32, single display.

1.5.2 Direct

Feedback for all bunches on, first coefficient set to 32767 (use command `caput IGPF:TEST:CSET0 32767`). Averaging factor of 4, dual display (magnitude and delay), marker at −3 dB from the maximum gain.

1.5.3 Filter

Filter coefficients generated with gain of 0.1, phase of 0, frequency set to $1/N_{\mathrm{taps}}$, maximum supported filter length. Dual display with magnitude and phase, port extension set to the delay measured earlier. Center frequency

at the revolution harmonic nearest to 15 MHz, revolution frequency span. Marker on the gain peak (upper sideband).

1.5.4 Downsampled filter

The same filter as above, processing downsampling set to 10. Frequency span of $f_{\mathrm{ref}}/10$. Marker on the upper sideband gain peak.

1.6 DAC response

Configure drive for $f_{\mathrm{clk}}/8$ or $f_{\mathrm{clk}}/4$ square wave for all bunches, disable feedback. Connect `DAC+` to SD-24 channel 0 and `DAC-` to 11801C trigger input. Record rise and fall times, peak-to-peak amplitude, overshoot and undershoot.

1.7 Instruments used

All instruments used for iGp12 testing are listed in Table 1.

Table 1: Instruments

Model	Description	Serial №	Cal. date/certificate
HP 8662A	Synthesized signal generator	2232A01056	2011-08-11/1466327
Agilent 8664A	Synthesized signal generator	3744A02491	2011-08-11/1466394
HP 4396A	Spectrum/network analyzer	3241J00268	2011-08-11/1466348
Tek11801C	Sampling scope mainframe	B030426	2011-08-11/1466413
Tek SD-24	20 GHz TDR sampling head	B022559	2011-08-11/1466390
SRS CG635	Clock generator	1459	2011-08-11/1466408

2 Measurements

Table 2: Measured parameters

Parameter	Value
Input -3 dB bandwidth (GHz)	1.27
Input full-scale level (dBm)	1.64
SFDR (dB)	74.0
SINAD (dB)	59.3
ENOB	9.6
Input rise time (ps)	353
Input fall time (ps)	342
Input overshoot (%)	21.9
Input undershoot (%)	23.8
Output rise time (ps)	373
Output fall time (ps)	390
Output amplitude (mVpp)	832
Output overshoot (%)	14.6
Output undershoot (%)	17.7
Group delay (ns)	1387

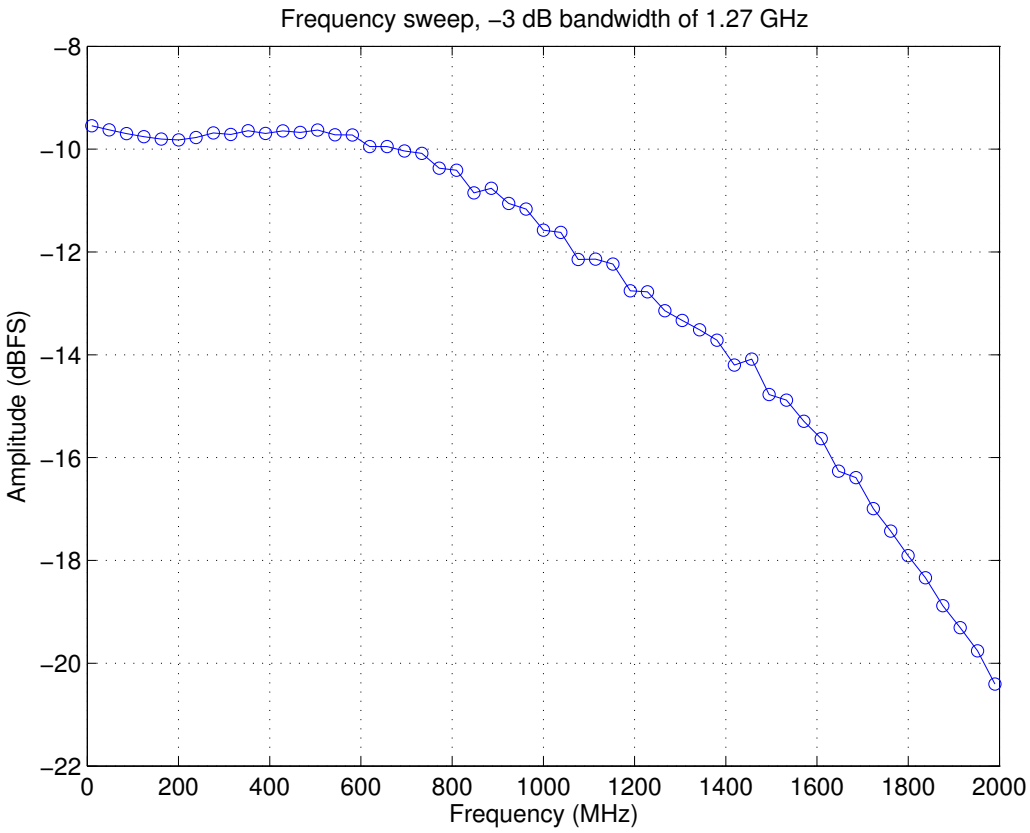

Figure 1: ADC frequency response

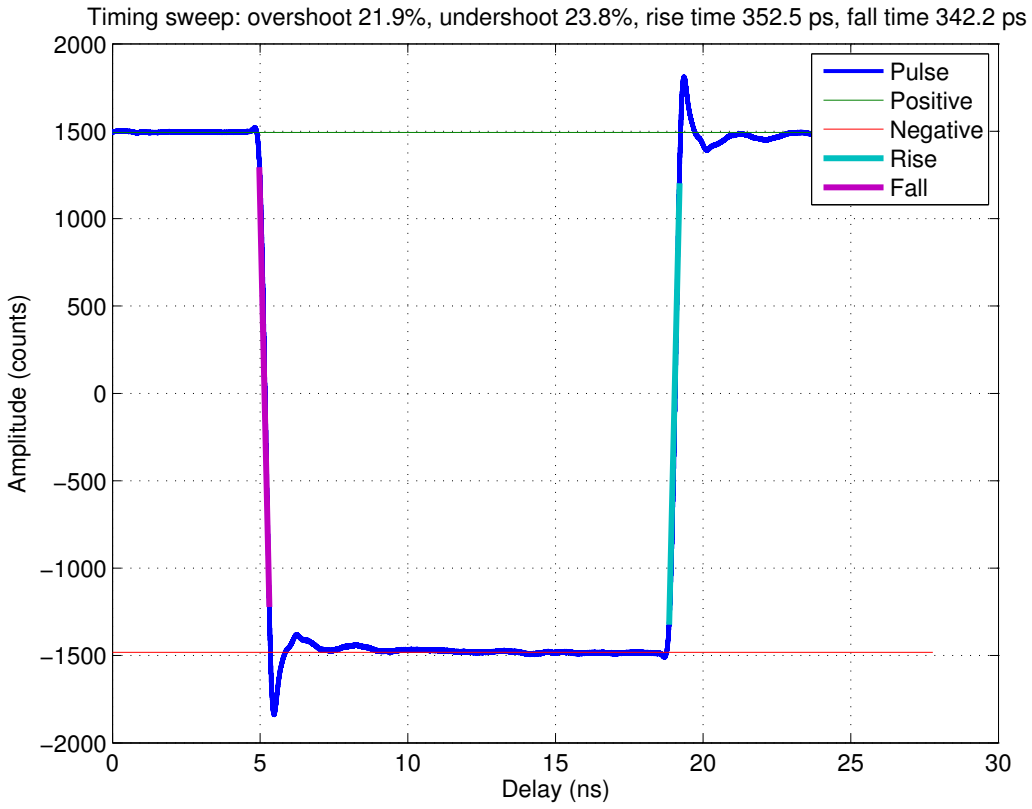

Figure 2: ADC step response

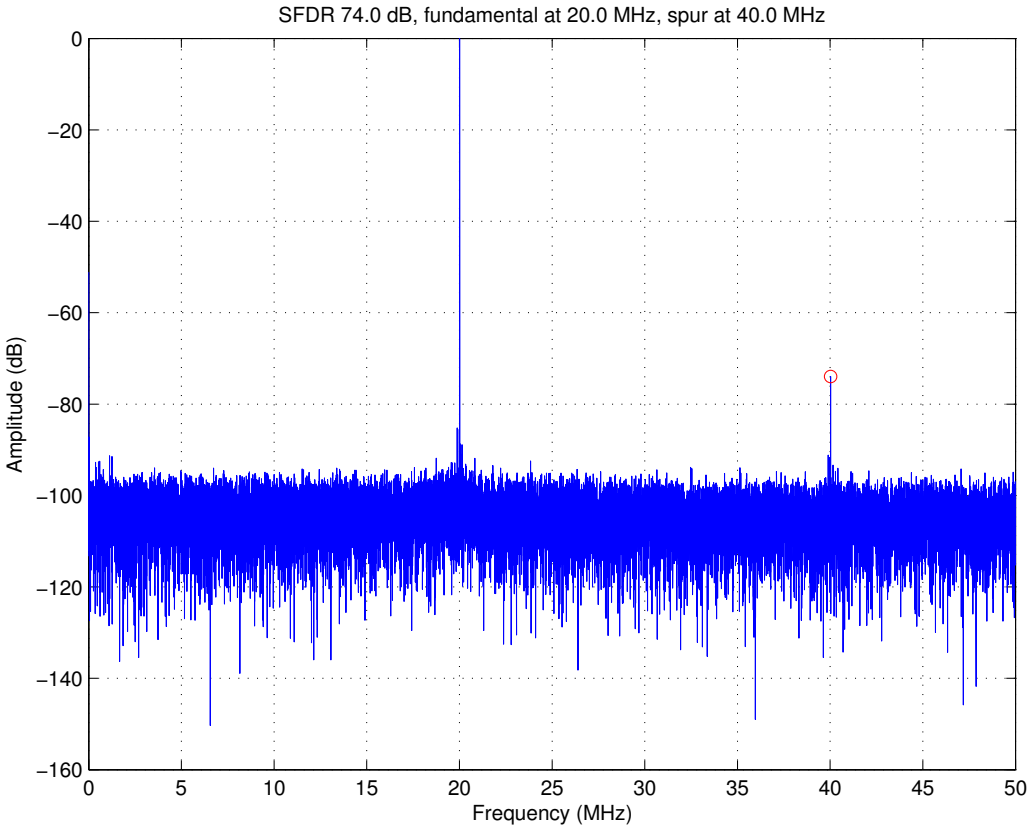

Figure 3: Spurious-free dynamic range

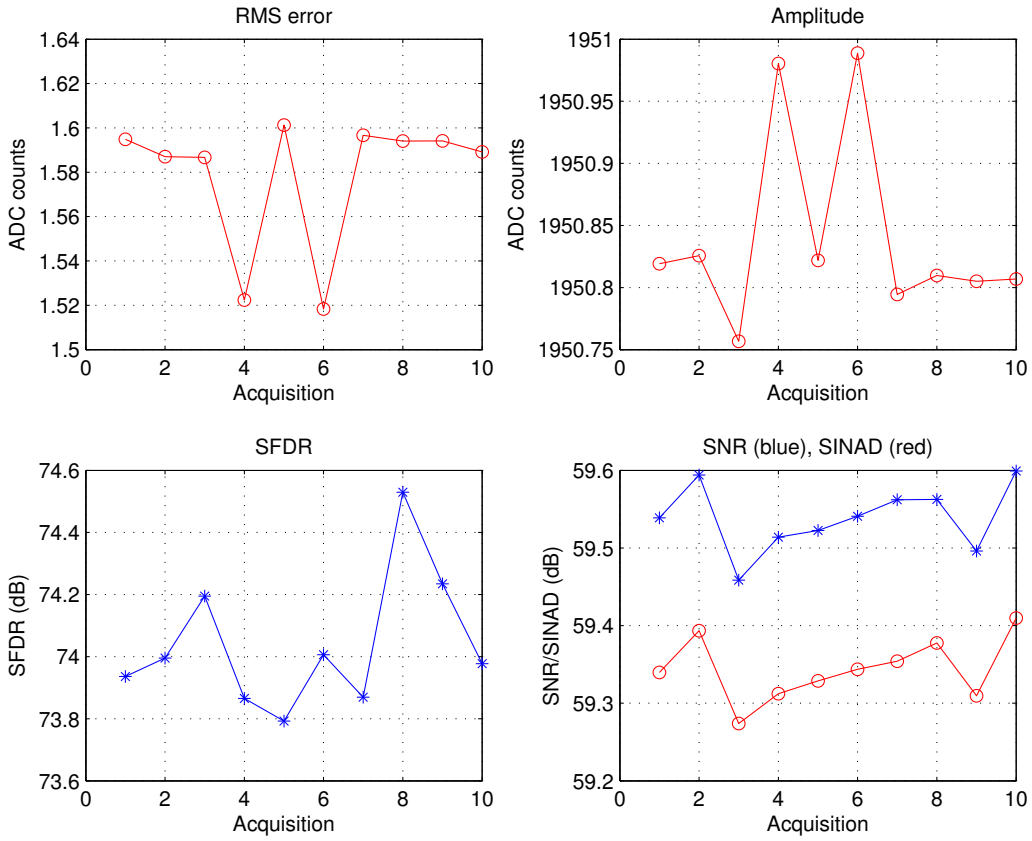

Figure 4: ADC tests: SNR, SFDR, SINAD, RMS error

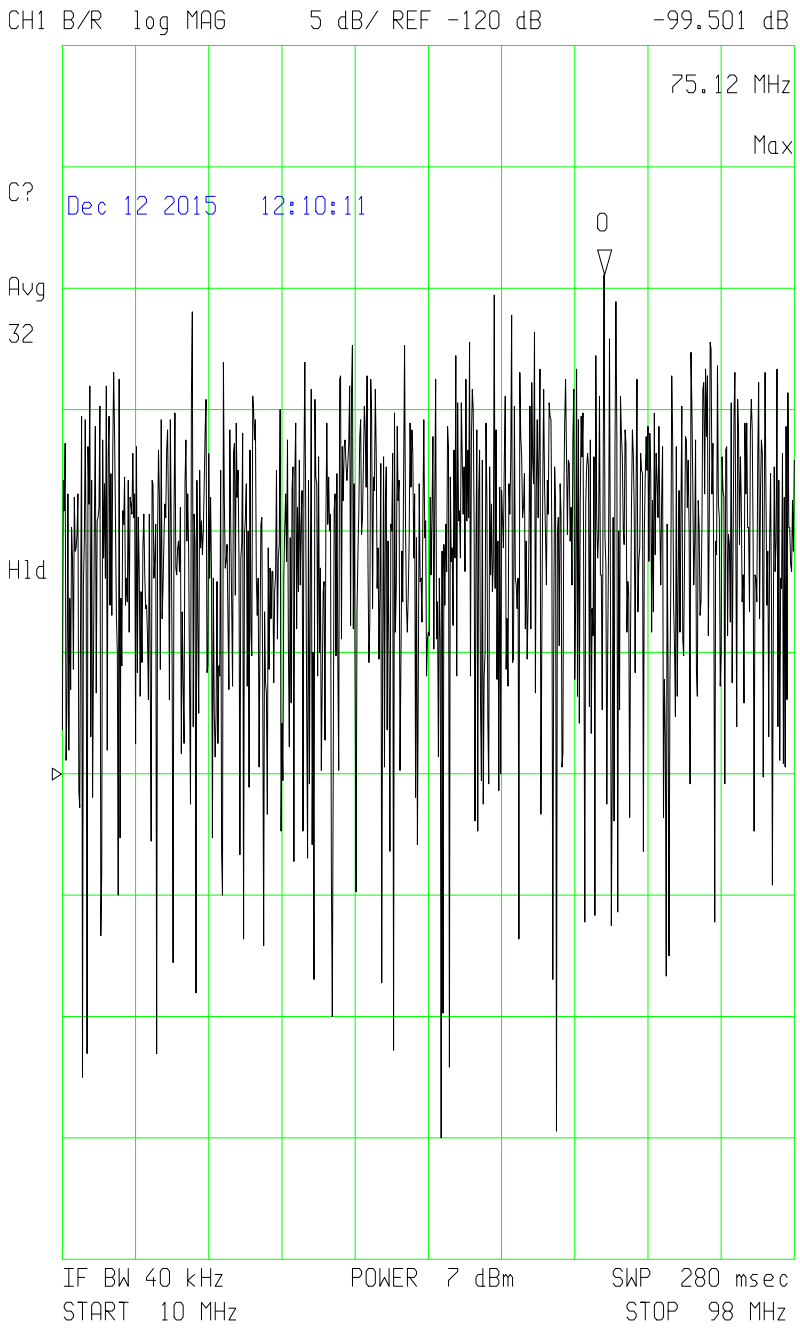

Figure 5: ADC to DAC coupling (feedback off)

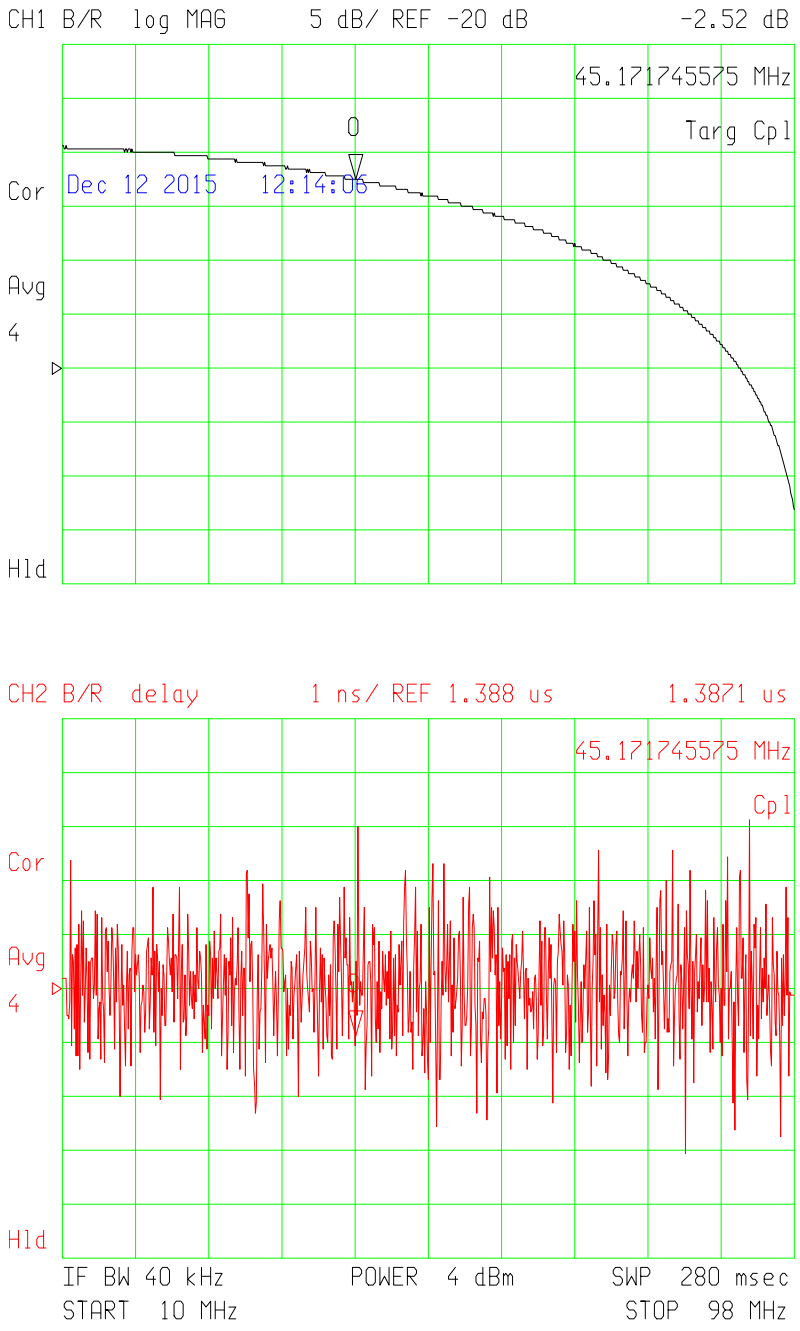

Figure 6: Through mode

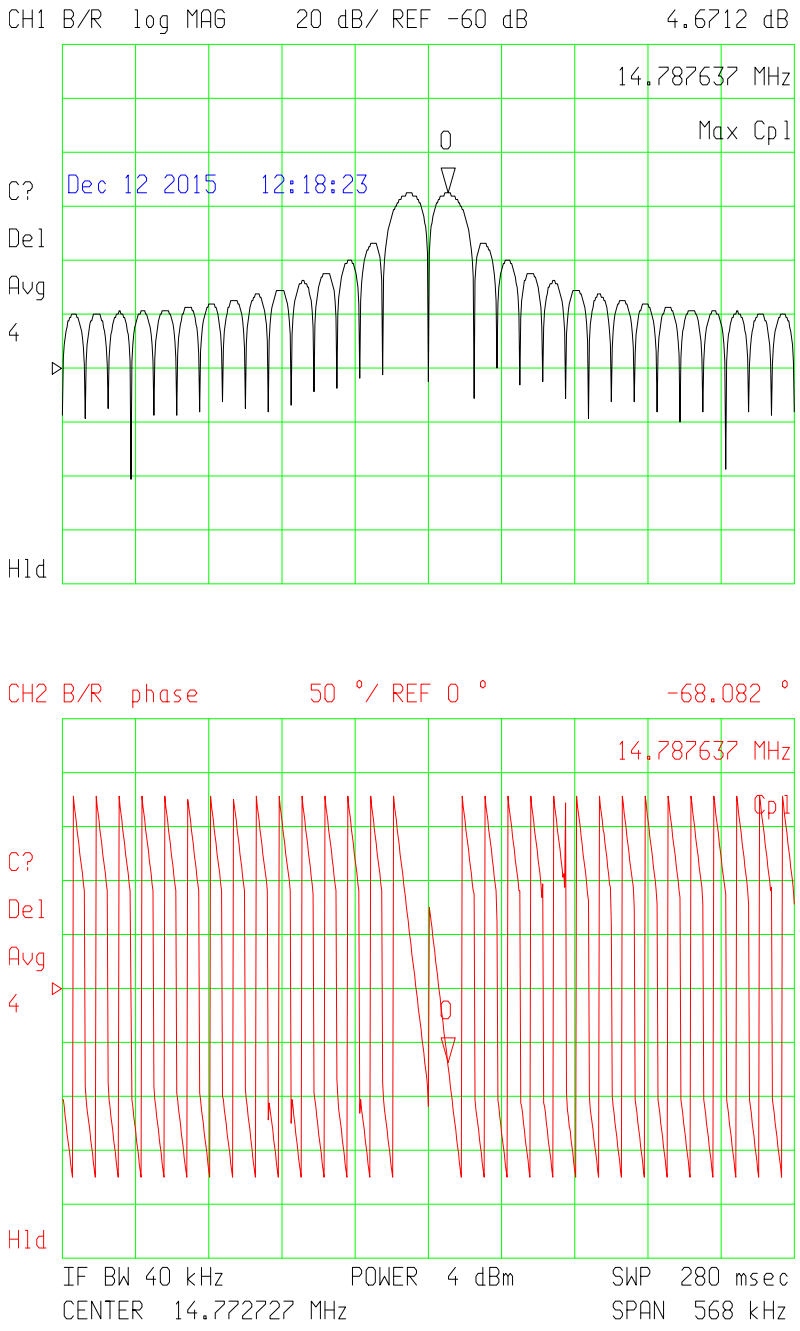

Figure 7: Filter, no downsampling

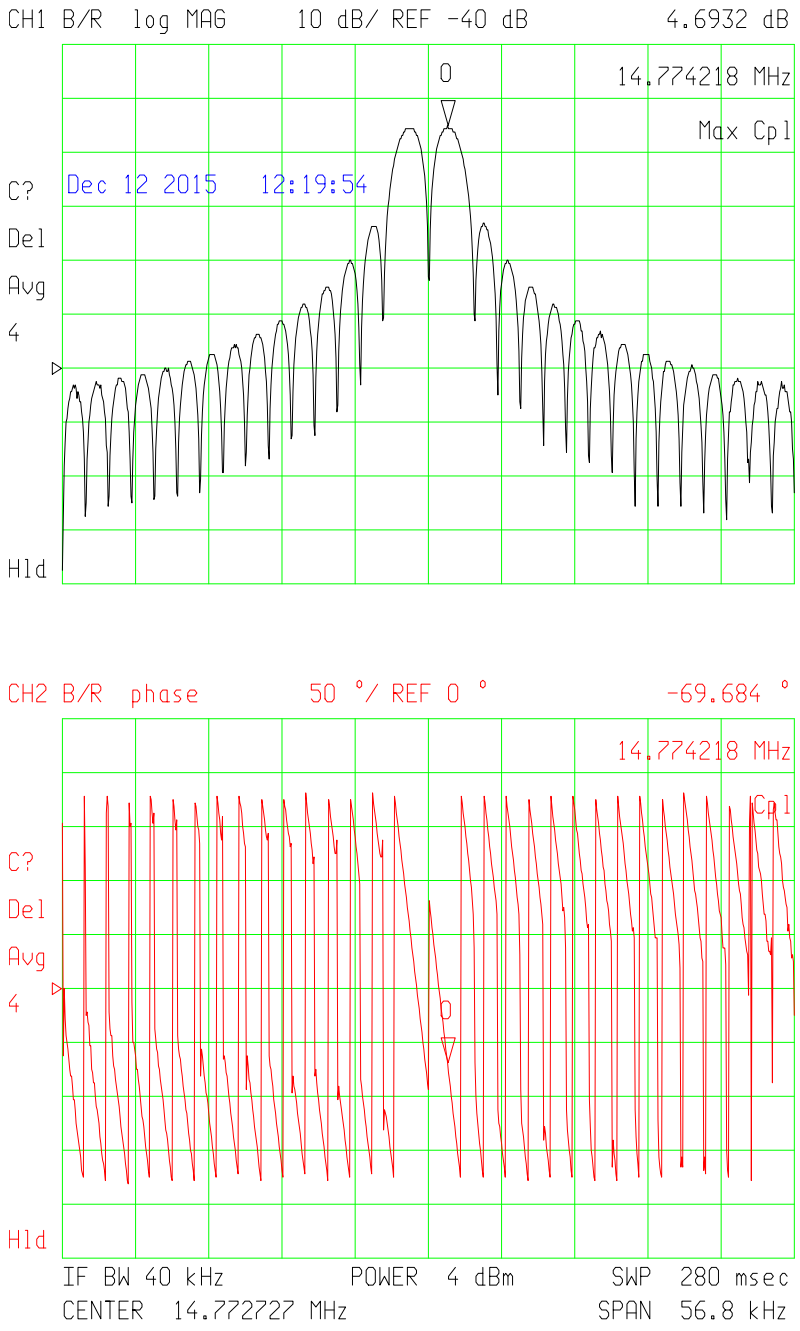

Figure 8: Filter, downsampling of 10