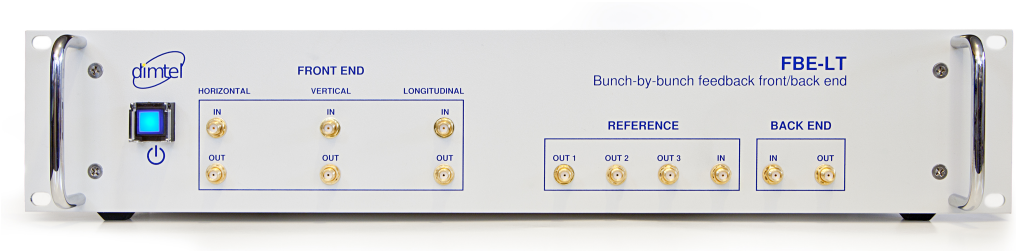

FBE-167LT Bunch-by-bunch Feedback Front/Back-End

Technical User Manual

Author:
Dmitry Teytelman

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Dimtel, Inc.
2059 Camden Avenue, Suite 136
San Jose, CA 95124
Phone: +1 650 862 8147
Fax: +1 603 218 6669
www.dimtel.com

Contents

1 Regulatory Compliance Information

This equipment requires a ground connection provided by the power source. The exposed metal parts of the unit are connected to the power ground to protect against electrical shock. Always use an outlet with properly connected protective ground.

FBE-167LT was designed and tested to operate safely under the following environmental conditions:

- indoor use;
- altitude to 2000 meters;
- temperatures from 5 to 40 °C;
- maximum relative humidity 80% for temperature 31 °C, decreasing linearly to 50% @ 40 °C;
- pollution category II;
- overvoltage category II;
- mains supply variations of ±10% of nominal.

FBE-167LT contains no user serviceable parts inside. Do not operate with the cover removed. Refer to qualified personnel for service.

NOTE: *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

NOTE: *This Class A digital apparatus complies with Canadian ICES-003. Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.*

2 Introduction

2.1 Delivery Checklist

1. FBE-167LT chassis;
2. AC power cord;
3. GPIO 68-pin male to 68-pin male cable;
4. User manual.

2.2 System Overview

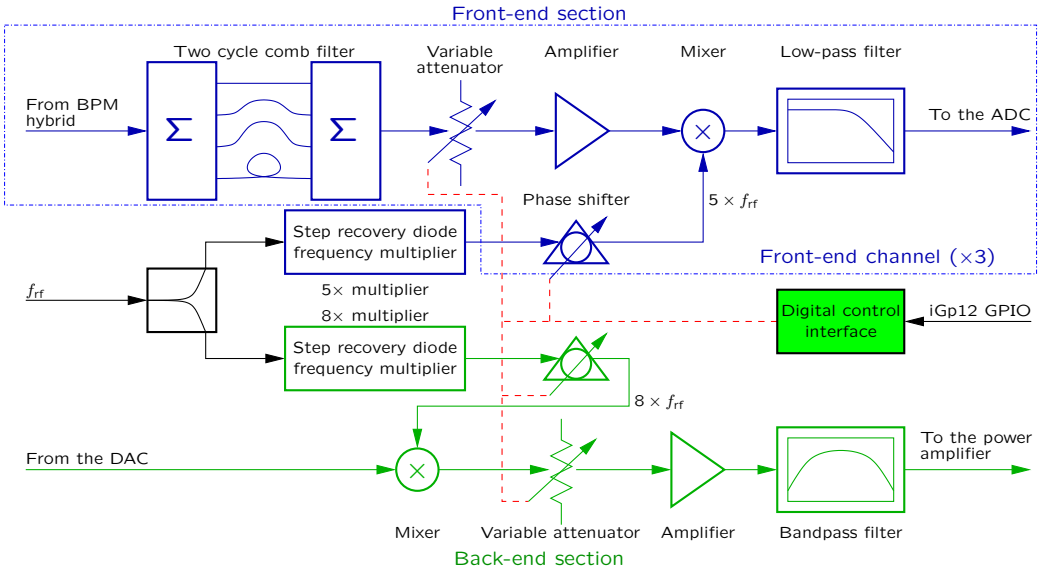

Figure 1: Bunch-by-bunch feedback front/back-end block diagram

The FBE-167LT RF signal processor incorporates front-end and back-end electronics for a complete bunch-by-bunch feedback system in a storage ring. The unit is equipped with three identical front-end channels — for processing horizontal, vertical, and longitudinal signals. Front-end channels are designed for converting the beam position monitor (BPM) output to the baseband signal which can be directly digitized by the iGp/iGp12. Each channel operates at 833 MHz and uses a 2-cycle comb filter to produce a detected pulse of 2.5 ns. The back-end channel upconverts the baseband

kick signal to 1332.8 MHz carrier for driving the power amplifier and the kicker. The FBE-167LT interfaces to the iGp/iGp12 digital general-purpose input/output (GPIO) port for control and monitoring. Control channels include front- and back-end attenuators and phase shifters and fan speed. Through the GPIO port, iGp/iGp12 is also able to read out the unique FBE-167LT serial number and to monitor the internal temperature.

2.3 Front Panel Features

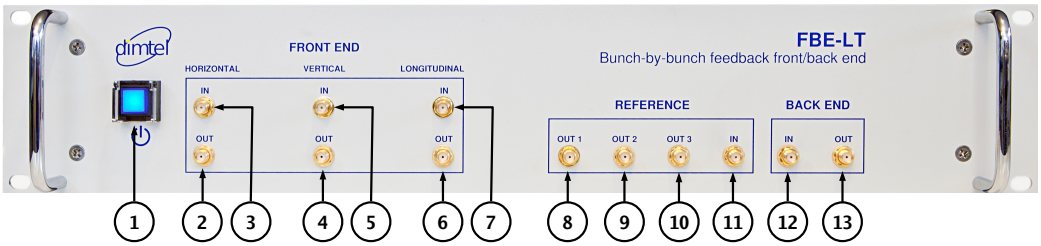

Figure 2: Front panel features

1) Power switch
This on-off lighted switch turns FBE-167LT on and off.

2) Horizontal front-end output
Baseband output to iGp/iGp12.

3) Horizontal front-end input
This input receives the beam signal from the BPM difference hybrid network. Maximum continuous wave (CW) level is 33 dBm. For typical beam signal this limitation can be expressed as maximum swing of 14 V.

4) Vertical front-end output
Baseband output to iGp/iGp12.

5) Vertical front-end input
This input receives the beam signal from the BPM difference hybrid network. Maximum CW level is 33 dBm. For typical beam signal this limitation can be expressed as maximum swing of 14 V.

6) Longitudinal front-end output
Baseband output to iGp/iGp12.

7) Longitudinal front-end input
This input receives the beam signal from the BPM combiner network. Maximum CW level is 33 dBm. For typical beam signal this limitation can be expressed as maximum swing of 14 V.

8–10) Reference outputs
Master oscillator outputs to baseband processors (iGp/iGp12). These outputs are 7 dB below the reference input level, nominally at −4 dBm.

11) Reference input

Master oscillator reference. This reference drives front and back-end local oscillators, as well as the outputs to iGp/iGp12. Nominal input level is 3 dBm.

12) Back-end input

This input should be driven by one of iGp/iGp12 high-speed digital-to-analog converter (DAC) outputs. Nominal swing expected at this input is ±250 mV. For iGp12 use a 4 dB attenuator.

7) Back-end output

Output to the power amplifier. At 0 dB back-end attenuation and full 250 mV baseband drive the output level is +5 dBm.

2.4 Rear Panel Features

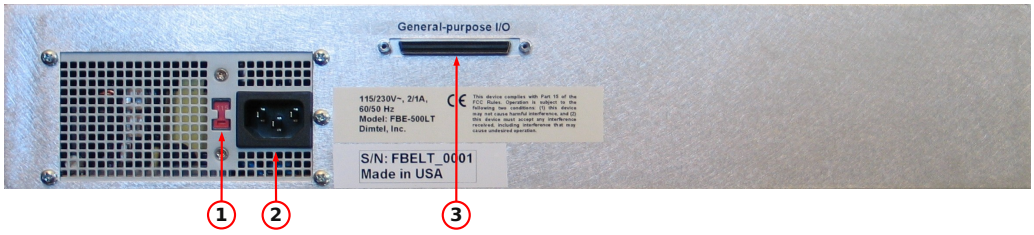

Figure 3: Rear panel features

1) **Voltage selection switch** Slide switch for selecting appropriate mains voltage: 115 or 230 V.
2) **Power entry socket** IEC-320 power input socket. Always use an outlet with properly connected protective ground.
3) **iGp/iGp12 interface** This 68-pin connector must be attached to the iGp/iGp12 for proper operation of the control elements within FBE-167LT.

2.5 Cooling Fan Filter Maintenance

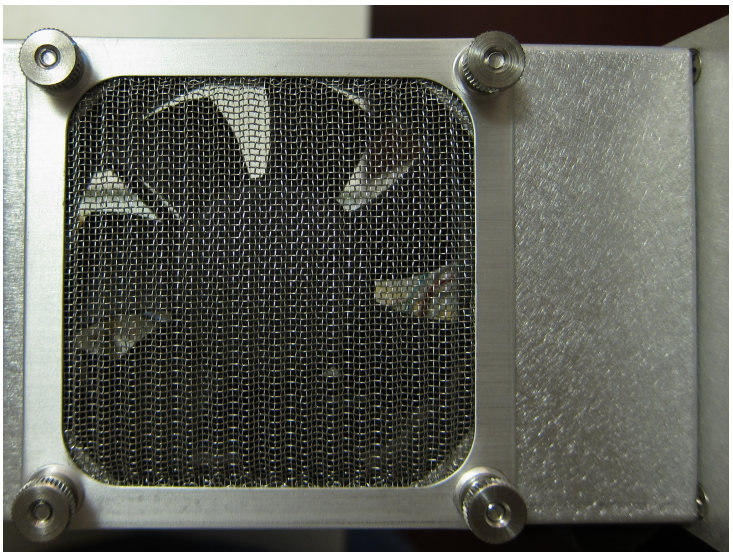

Figure 4: Fan filter mounted using four thumb nuts

Cooling fan is located on the left side of the FBE-167LT. A stainless steel mesh filter is mounted externally with four thumb nuts.

WARNING: Fan filter protects the system from contamination. Operating the unit without the filter can lead to overheating as well as to premature failure of the cooling fans.

WARNING: Before performing any work on the fan filter, power down the system and unplug the AC power cord. Fan blades are exposed when the filter is removed.

The filter should be periodically serviced to maintain adequate air flow. Vacuuming, washing or replacement are the acceptable maintenance options. Replacement filter is manufactured by Qualtek Electronics Corporation, part number 06325-M.

In order to remove the filter, undo the four thumb nuts. If filter servicing involves washing, make sure the filter is completely dry before reinstallation. To reinstall, orient the filter so that the mesh corrugations are vertical and slide it onto the mounting studs. Reinstall and hand tighten the thumb screws.

2.6 Getting Started

In this section we will present a quick step-by-step guide to get your new RF front/back-end processor running in a minimal (single-channel) configuration.

WARNING: Before connecting power to the unit make sure the voltage selection switch (Fig. 3, item 1) is in the correct position (115 or 230 V).

WARNING: Signals beyond +33 dBm CW or 14 V peak can permanently damage the front-end input circuitry! Before connecting to FBE-167LT, measure BPM signals using a high-speed oscilloscope at maximum bunch currents to determine the necessary input attenuation level.

1. Configure voltage selection switch (Fig. 3, item 1). Mains supply requirements for the FBE-167LT are listed in Table 4;
2. Connect radio frequency (RF) clock at 3 dBm nominal level (Fig. 2, item 5);
3. Connect the reference output (Fig. 2, item 8) to the CLK input of the iGp/iGp12;
4. Terminate unused reference outputs with wideband 50 Ω SMA terminators;
5. Connect the front-end input (Fig. 2, item 3, 5, or 7) to the beam signal at the appropriate level;
6. Connect the front-end output (Fig. 2, item 2, 4, or 6) to the IN+ or IN- of the iGp/iGp12. Terminate the unused iGp/iGp12 input with a wideband 50 Ω SMA terminator;
7. Connect the back-end input (Fig. 2, item 6) to the OUT+ or OUT- of the iGp/iGp12. Terminate the unused iGp/iGp12 output with a wideband 50 Ω SMA terminator. When using iGp12, place a 4 dB attenuator between the DAC output and the back-end input;
8. Connect the back-end output (Fig. 2, item 7) to the power amplifier input;
9. Using the supplied 68-pin GPIO cable connect the iGp/iGp12 interface (Fig. 3, item 3) to the GPIO connector on the iGp/iGp12;

10. Push the power button (Fig 2, item 1) to turn on the system;

At this point your system is ready for use in beam diagnostics and feedback. The system must be appropriately phased and timed to the beam. This ensures proper phase detection in the front-end and correct sampling of the detected signal as well as the correct phase of the kick signal and its timing relative to the bunch arrival in the kicker.

3 Setup

As mentioned in Subsection 2.6, the FBE-167LT must be properly phased and timed to the beam. In this section several possible methods for achieving proper timing and phasing will be described. Let us start with the front-end setup.

WARNING: The FBE-167LT must be operated for at least two hours in the installation environment to achieve thermal equilibrium. Do not perform phase-sensitive front- and back-end adjustments before the equilibrium has been achieved.

3.1 Front-end

WARNING: Front-end circuitry is sensitive to peak and average signal levels. Absolute maximum input level is +33 dBm CW or 14 V peak. However within these ranges internal amplifier damage is possible if the front-end attenuator is set too low for the input signal level! Before changing per bunch currents set the front-end attenuator to nominal attenuation at that bunch current.

In order to time the front-end to the beam, a single-bunch filling pattern should be used. With a single bunch filled, connect the front-end output to a scope and adjust front-end phase for amplitude detection, producing a large pulse in the baseband signal. Next, connect the signal to the iGp/iGp12 input and adjust the timing in 100 ps steps (10 units of 10 ps delay line) to produce maximum displacement in the mean offset of one bunch. This operation results in somewhat coarse front-end timing. For more precise adjustment one can use `sweep.sh` script supplied with iGp/iGp12.

Once the front-end is timed, adjust the front-end phase for amplitude detection in the horizontal and vertical channels and for phase detection in the longitudinal channel.

3.2 Back-end

Back-end timing consists of two parts: phasing the back-end local oscillator to produce maximum kick, and adjusting kick envelope timing to line up the single-bunch kick with the beam.

In the first step, configure the iGp/iGp12 to generate sinewave drive at the synchrotron frequency using the turn-by-turn option of the drive generator. At this point all bunches should be driven. Next, adjust back-end phase to produce maximum longitudinal excitation, as measured by the iGp/iGp12 or by an external instrument. Drive amplitude might need to be reduced to precisely find the optimal phase.

At this point we need to determine which bunch in the iGp/iGp12 processing is lined up with the beam. To do so, bisection is typically used. Initially our bunch drive pattern might look like `1:64`. Select the first half of the ring using `1:32`. If the beam is still excited one of the first 32 bunches in iGp/iGp12 processing coincides with the beam in the kicker. Continue the bisection until one bunch is identified. At this point one can adjust the output (one-turn) delay so that the excited bunch number agrees with the bunch number seen in the front-end. Once such agreement is reached the back-end can be considered coarsely timed. For finer timing the iGp/iGp12 output timing must be adjusted in sub-RF-period steps to maximize the beam response.

4 Specifications

Table 1: General specifications

Parameter	Definition
Operating frequency	166.6 MHz
RF input level	3 ± 1 dBm
Reference output level	-7 dB relative to the input
Temperature sensing resolution	0.0625 °C
Fan speed control range	1600–4000 RPM
Unique ID	Provided by Maxim DS1822 device
Chassis	2U 19” rackmount, 16” deep

Table 2: Front-end specifications

Parameter	Definition
Detection frequency	833 MHz
Maximum operating input level	9.3 V peak
Absolute maximum input level	14 V peak
Attenuation range	0–31.5 dB
Output level at 1 dB compression	0 dBm
3 dB bandwidth	250 MHz
Baseband pulse width	2.5 ns
Phase shifter range	$>$ 360 degrees
Phase shifter resolution	$<$ 0.2 degrees/step
Input signal range	-70 to -17 dBm
Channel to channel isolation	50 dB
Input/output impedance	50 Ω

NOTE: *Input signal range is measured with the attenuation set to* 0 *dB. Input signal at positive 20 MHz offset from 833 MHz is adjusted to span the range from iGp12 full scale down to 3 dB SNR.*

Table 3: Back-end specifications

Parameter	Definition
Modulation frequency	1332.8 MHz
Input level	±250 mV
Attenuation range	0–31.5 dB
Maximum output level (DC input of 250 mV, 3 dBm reference)	+5 dBm
Output filter	5^{th} order Bessel band-pass
Output bandwidth	250 MHz
Phase shifter range	$>$ 360 degrees
Phase shifter resolution	$<$ 0.2 degrees/step

NOTE: *Back-end Bessel band-pass is centered at* $8.5 \times f_{\text{rf}}$. *Overall back-end response is from* $8 \times f_{\text{rf}}$ *to* $9 \times f_{\text{rf}}$.

Table 4: Input Power Requirements

Parameter	Definition
Input voltage	115/230 VAC
Input current	2/1 A
Frequency	60/50 Hz
Voltage selection	Switch
Low voltage range	104–126 V
High voltage range	207–253 V

5 Warranty and Support

5.1 Warranty

Dimtel Inc. warranties this product for a period of one year from the date of shipment against defective workmanship or materials. This warranty excludes any defects, failures or damage caused by improper use or inadequate maintenance, installation or repair performed by Customer or a third party not authorized by Dimtel, Inc. Warrantied goods will be either repaired or replaced at the discretion of Dimtel, Inc. The above warranties are exclusive and no other warranty, whether written or oral, is expressed or implied.

5.2 Support

Dimtel Inc. will provide technical support for the product free of charge for a period of one year from the date of shipment. Such support is defined to include:

- Gain partitioning;
- System interconnection issues;
- iGp/iGp12 interface support.

Free of charge technical support specifically excludes:

- Commissioning with beam;
- Feedback algorithm development and testing;
- Beam dynamics characterization;
- Operational support related to dynamic system operation.

6 Appendix A: Control Interface

External control and monitoring of FBE-167LT is done through a 68-pin connector mounted on the rear-panel. Most bottom row pins (36–68) are grounded as well as pin 17 on the top row. Interface signals use 17 pins on the top row.

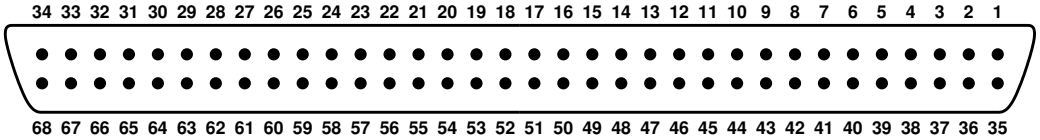

Figure 5: Pin numbering for digital interface connector

Figure 5 shows the pin numbering for the digital interface connector. Pin definitions are listed in Table 5.

Table 5: Digital interface pinout

Pin number	Definition	V_{IL}, V	V_{IH}, V	V_{min}, V	V_{max}, V
1	N/C				
2	SCLK_HMC	0.8	2.0	0	5.0
3	SDATA_HMC	0.8	2.0	0	5.0
4	LE_LONG	0.8	2.0	0	5.0
5	CS_DAC	0.8	2.0	0	5.0
6	LE_BE	0.8	2.0	0	5.0
7	DS1822_DQ	-0.3	2.2	0	3.3
8	SDATA_OUT_LONG			0	5.0
9	SDATA_OUT_BE			0	5.0
10	SDATA_OUT_VERT			0	5.0
11	SDATA_OUT_HOR			0	5.0
12	LE_VERT	0.8	2.0	0	5.0
13	LE_HOR	0.8	2.0	0	5.0
14	FAN_TACH	open collector			
15	MOD_SENSE	grounded			
16	SDATA_DAC	0.8	2.4	0	5.0
17	GND				
18	SCLK_DAC	0.8	2.4	0	5.0

Continued on next page

Table 5 – continued from previous page

Pin number	Definition	V_{IL}, V	V_{IH}, V	V_{min}, V	V_{max}, V
19–34	Reserved				
35	N/C				
36–68	GND				

Digital interface to FBE-167LT can be split into four groups:

1. Serial peripheral interface (SPI) interface to four Hittite/Analog Devices HMC542BLP4E digital attenuators;
2. SPI interface to Maxim MAX5590 octal DAC;
3. 1-Wire interface to Maxim DS1822 digital thermometer;
4. Chassis fan tachometer output.

One signal that does not belong to any of the above four groups is the modification sense signal, `MOD_SENSE`, pin 15. This signal is used to distinguish older interface revisions (floating) and modern version (grounded). In iGp12, the controller senses this signal and activates the appropriate interface logic. The older interface has been deprecated in 2016, so one can fairly safely assume the FBE-167LT implements the modern interface version described in this document.

Four groups listed above are described in detail the following subsections.

6.1 Attenuator control

FBE-167LT includes four HMC542BLP4E[1] digital attenuators, one in each of three front end channels and one in the back end. All input signals have a series ferrite bead (BLM18BD102SN1D) and are internally buffered by 74HCT244. Output signals have a 360 Ω series damping resistor and a ferrite bead. Attenuator datasheet specifies maximum serial clock rate of 30 MHz. Interface controller in iGp12 uses 1.5 MHz serial clock for robustness and reduced EMI. Signals, used for attenuator control interface are summarized in Table 6. Signal direction is specified from the FBE-167LT perspective.

Two signals are shared by all four attenuators — `SCLK_HMC` and `SDATA_HMC`. Eight bit control word is shifted into all HMC542BLP4E devices at the same

[1] Refer to Analog Devices, Inc. website for detailed programming information.

Table 6: Attenuator control interface

Signal	Pin	Direction	Description
SLCK_HMC	2	input	Common serial clock
SDATA_HMC	3	input	Common serial data input
LE_LONG	4	input	Longitudinal front end latch enable
LE_VERT	12	input	Vertical front end latch enable
LE_HOR	13	input	Horizontal front end latch enable
LE_BE	6	input	Back end latch enable
SDATA_OUT_LONG	8	output	Longitudinal shift register output
SDATA_OUT_VERT	10	output	Vertical shift register output
SDATA_OUT_HOR	11	output	Horizontal shift register output
SDATA_OUT_BE	9	output	Back end shift register output

time. By pulsing one of four latch enable controls high, the setting is latched in the corresponding attenuator. Serial shift register outputs are also available and can be used to verify that signals are correctly propagating through each attenuator.

6.2 Eight channel DAC

An eight channel 12-bit DAC (MAX5590[2]) is used in FBE-167LT to control four phase shifters (three front end, one back end) and fan speed. Table 7 lists the interface pins used to control MAX5590 DAC.

Table 7: Eight channel DAC interface

Signal	Pin	Direction	Description
SLCK_DAC	18	input	Serial clock, MAX5590 input SCLK, pin 10
SDATA_DAC	16	input	Serial data, MAX5590 input DIN, pin 11
CS_DAC	5	input	Chip select, MAX5590 input $\overline{\text{CS}}$, pin 9

Channel function assignments are shown in Table 8. Analog phase shifters in FBE-167LT have non-linear response to control voltage, with steeper phase shift sensitivity at low voltages and flatter response at high settings. Full span of 0 to 4095 counts typically corresponds to 380–440° range of carrier phase

[2]Refer to Maxim Integrated website for detailed programming information

shift. Refer to factory test results to obtain precise phase shifter ranges for individual channels on a given unit.

Table 8: DAC channel assignment

Output	MAX5590 pin	Function
OUTA	3	Fan speed control
OUTB	5	Unused
OUTC	6	Unused
OUTD	7	Unused
OUTE	18	Back end phase shifter
OUTF	19	Horizontal front end phase shifter
OUTG	20	Vertical front end phase shifter
OUTH	22	Longitudinal front end phase shifter

Fan speed control output is inverted in hardware, with the setting of 0 corresponding to the maximum fan speed. Fan drive voltage is related to DAC setting N_{DAC} as follows:

$$V_{\mathrm{fan}} = V_{\mathrm{max}} - (V_{\mathrm{max}} - V_{\mathrm{min}})\frac{N_{\mathrm{DAC}}}{4096}$$

Typical values for minimum and maximum voltages are 5 and 11 V respectively. When FBE-167LT is powered on, the output of the DAC defaults to 0, so the fan operates at maximum speed. Adjustments of fan speed should always be done in closed-loop, in response to temperature measurements. Running FBE-167LT with insufficient cooling for the ambient conditions can lead to increased component failure rates.

6.3 DS1822 interface

A 1-Wire digital thermometer DS1822[3] from Maxim Integrated serves several functions in the FBE-167LT. It provides a unique host-accessible serial number, that can be used, if desired, to apply device-specific calibration curves[4]. The most important function of DS1822, however, is temperature

[3]Refer to Maxim Integrated website for detailed programming information.

[4]For example, phase shifter linearization can be automatically applied based on the serial number.

measurement. Periodic sampling of FBE-167LT internal temperature is used in iGp12 experimental physics and industrial control system (EPICS) input-output controller (IOC) to perform closed-loop temperature stabilization via cooling fan speed control. Same functionality, of course, can be implemented in a standalone controller.

1-Wire thermometer is internally powered by 3.3 V supply. Bidirectional signal `DS1882_DQ` has an internal 4.7 kΩ pullup to 3.3 V supply.

6.4 Chassis fan monitoring

Fan tachometer signal `FAN_TACH` is an open-collector output. With an external pullup a square wave signal is generated by the rotating fan. Two periods of the square wave correspond to one revolution of the rotor. To calculate fan rotation speed in RPM, measured signal frequency must be multiplied by 30.

7 Glossary

Glossary

beam position monitor (BPM)

An RF structure that couples to the beam in the accelerator. The output signal of such a structure allows measurement of the transverse or the longitudinal beam position. 3, 5, 9

continuous wave (CW)

A signal of constant amplitude and frequency. 5, 9, 10

digital-to-analog converter (DAC)

A hardware device to convert a sequence of digital codes to corresponding analog voltages or currents. 6, 16–18

experimental physics and industrial control system (EPICS)

A set of software tools and applications used to develop distributed soft real-time control systems. 18

general-purpose input/output (GPIO)

A 32-bit wide digital input/output port of the iGp/iGp12. 3, 9

input-output controller (IOC)

An embedded computer used to interface the hardware to the control system. 18

radio frequency (RF)

In the accelerator context, a constant frequency constant amplitude signal derived from or phase locked to the storage ring master oscillator. 9, 12

serial peripheral interface (SPI)

A synchronous serial interface consisting of at least three signals: clock, data output from master to slave, and select or latch enable. 16