FBE-500L Longitudinal RF Signal Processor

Technical User Manual

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1 Regulatory Compliance Information

This equipment requires a ground connection provided by the power source. The exposed metal parts of the unit are connected to the power ground to protect against electrical shock. Always use an outlet with properly connected protective ground.

FBE-500L was designed and tested to operate safely under the following environmental conditions:

- indoor use;
- altitude to 2000 meters;
- temperatures from 5 to 40 °C;
- maximum relative humidity 80% for temperature 31 °C, decreasing linearly to 50% @ 40 °C;
- pollution category II;
- overvoltage category II;
- mains supply variations of ±10% of nominal.

FBE-500L contains no user serviceable parts inside. Do not operate with the cover removed. Refer to qualified personnel for service.

2 Introduction

2.1 Delivery Checklist

1. FBE-500L chassis;
2. AC power cord;
3. GPIO 68-pin male to 68-pin male cable;
4. User manual.

2.2 System Overview

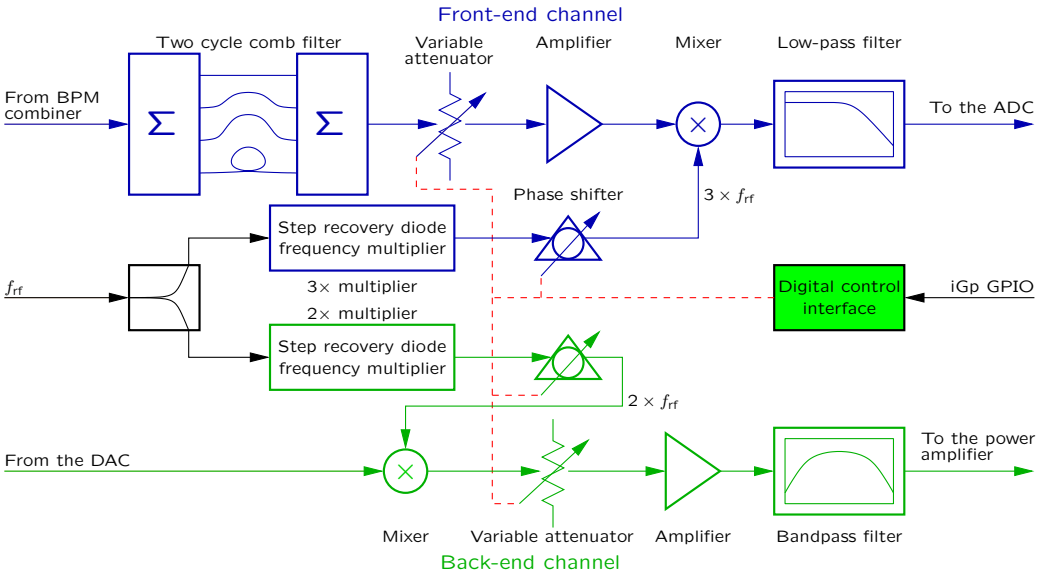

Figure 1: Longitudinal RF signal processor block diagram

The FBE-500L RF signal processor incorporates front-end and back-end electronics for a longitudinal bunch-by-bunch feedback system. The front-end channel is designed for converting the beam position monitor (BPM) output to the baseband signal which can be directly digitized by the integrated gigasample processor (iGp). It operates at 1500 MHz and uses a 2-cycle comb filter to produce a detected pulse of 1.3 ns. The back-end channel upconverts the baseband kick signal to 1000 MHz carrier for driving the

power amplifier and the kicker. The FBE-500L interfaces to the iGp digital general-purpose input/output (GPIO) port for control of front- and back-end attenuators and phase shifters.

2.3 Front Panel Features

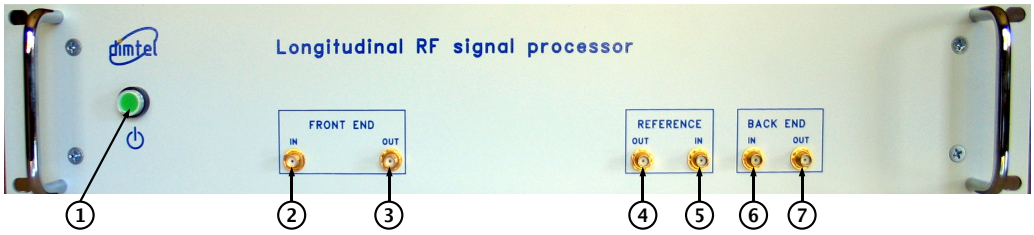

Figure 2: Front panel features

1) Power switch This on-off lighted switch turns FBE-500L on and off.

2) Front-end input This input receives the beam signal from a BPM combiner. Maximum continuous wave (CW) level is 33 dBm. For typical beam signal this limitation can be expressed as maximum swing of 14 V.

3) Front-end output Phase detector output to iGp.

4) Reference output Master oscillator output to iGp. This output is 4 dB below the input level, nominally at −4 dBm.

5) Reference input Master oscillator reference. This reference drives front and back-end local oscillators, as well as the output to iGp. Nominal input level is 0 dBm.

6) Back-end input This input should be directly driven by one of iGp high-speed digital-to-analog converter (DAC) outputs. Nominal swing expected at this input is ±250 mV.

7) Back-end output Output to the power amplifier. At 0 dB back-end attenuation and full 250 mV baseband drive the output level is 10 dBm.

2.4 Rear Panel Features

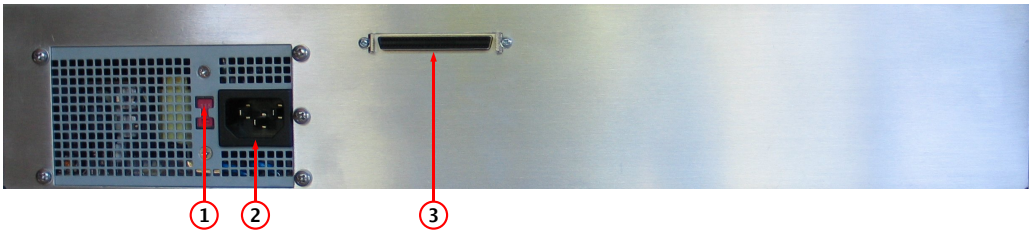

Figure 3: Rear panel features

1) Voltage selection switch Slide switch for selecting appropriate mains voltage: 115 or 230 V.

2) Power entry socket IEC-320 power input socket. Always use an outlet with properly connected protective ground.

3) iGp interface This 68-pin connector must be attached to the iGp for proper operation of the control elements within FBE-500L.

2.5 Getting Started

In this section we will present a quick step-by-step guide to get your new RF signal processor running in a minimal configuration.

WARNING: Before connecting power to the unit make sure the voltage selection switch (Fig. 3, item 1) is in the correct position (115 or 230 V).

WARNING: Signals beyond +33 dBm CW or 14 V peak can permanently damage the front-end input circuitry! Before connecting to FBE-500L, measure BPM signals using a high-speed oscilloscope at maximum bunch currents to determine the necessary input attenuation level.

1. Configure voltage selection switch (Fig. 3, item 1). Mains supply requirements for the iGp are listed in Table 4;
2. Connect radio frequency (RF) clock at 0 dBm nominal level (Fig. 2, item 5);
3. Connect the reference output (Fig. 2, item 4) to the CLK input of the iGp;
4. Connect the front-end input (Fig. 2, item 2) to the beam signal at the appropriate level;
5. Connect the front-end output (Fig. 2, item 3) to the IN+ or IN- of the iGp. Terminate the unused iGp input with a wideband 50 Ω SMA terminator;
6. Connect the back-end input (Fig. 2, item 6) to the OUT+ or OUT- of the iGp. Terminate the unused iGp output with a wideband 50 Ω SMA terminator;
7. Connect the back-end output (Fig. 2, item 7) to the power amplifier input;
8. Using the supplied 68-pin GPIO cable connect the iGp interface (Fig. 3, item 3) to the GPIO connector on the iGp;
9. Push the power button (Fig 2, item 1) to turn on the system;

At this point your system is ready for use in beam diagnostics and feedback. The system must be appropriately phased and timed to the beam. This ensures proper phase detection in the front-end and correct sampling of the detected signal as well as the correct phase of the kick signal and its timing relative to the bunch arrival in the kicker.

3 Setup

As mentioned in Subsection 2.5, the FBE-500L must be properly phased and timed to the beam. In this section several possible methods for achieving proper timing and phasing will be described. Let us start with the front-end setup.

WARNING: The FBE-500L must be operated for at least two hours in the installation environment to achieve thermal equilibrium. Do not perform phase-sensitive front- and back-end adjustments before the equilibrium has been achieved.

3.1 Front-end

WARNING: Front-end circuitry is sensitive to peak and average signal levels. Absolute maximum input level is +33 dBm CW or 14 V peak. However within these ranges internal amplifier damage is possible if the front-end attenuator is set too low for the input signal level! Before changing per bunch currents set the front-end attenuator to nominal attenuation at that bunch current.

In order to time the front-end to the beam a single-bunch filling pattern should be used. With a single bunch filled, connect the front-end output to a scope and adjust front-end phase for amplitude detection, producing a large pulse in the baseband signal. Next, connect the signal to the iGp input and adjust the timing in 100 ps steps (10 units of 10 ps delay line) to produce maximum displacement in the mean offset of one bunch. This operation results in somewhat coarse front-end timing. For more precise adjustment one can use `fe_timing` MATLAB script.

Once the front-end is timed, adjust the front-end phase to minimize the DC offset of the filled bunch. At this point the front-end is set up for phase detection and ready to acquire the beam signals.

3.2 Back-end

Back-end timing consists of two parts: phasing the back-end local oscillator to produce maximum kick, and adjusting kick envelope timing to line up the single-bunch kick with the beam.

In the first step, configure the iGp to generate sinewave drive at the synchrotron frequency using the turn-by-turn option of the drive generator. At this point all bunches should be driven. Next, adjust back-end phase to produce maximum longitudinal excitation, as measured by the iGp or by an external instrument. Drive amplitude might need to be reduced to precisely find the optimal phase.

At this point we need to determine which bunch in the iGp processing is lined up with the beam. To do so, bisection is typically used. Initially our bunch drive pattern might look like `1:64`. Select the first half of the ring using `1:32`. If the beam is still excited one of the first 32 bunches in iGp processing coincides with the beam in the kicker. Continue the bisection until one bunch is identified. At this point one can adjust the output (one-turn) delay so that the excited bunch number agrees with the bunch number seen in the front-end. Once such agreement is reached the back-end can be considered coarsely timed. For finer timing the iGp output timing must be adjusted in sub-RF-period steps to maximize the beam response.

4 Specifications

Table 1: General specifications

Parameter	Definition
Operating frequency	500 MHz
RF input level	0 ± 1 dBm
Reference output level	-4 dB relative to the input

Table 2: Front-end specifications

Parameter	Definition
Detection frequency	1500 MHz
Maximum operating input level	9.3 V peak
Absolute maximum input level	14 V peak
Attenuation range	0–31.5 dB
Nominal output	190 mV peak-to-peak (-10.4 dBm)
3 dB bandwidth	500MHz
Baseband pulse width	1.9 ns
Phase shifter range	$>$ 360 degrees
Phase shifter resolution	$<$ 0.1 degrees/step

Table 3: Back-end specifications

Parameter	Definition
Modulation frequency	1000 MHz
Input level	±250 mV
Attenuation range	0–31.5 dB
Maximum output level (DC input of 250 mV, 0 dBm reference)	10 dBm
Output filter	5^{th} order Bessel band-pass
Output bandwidth	600 MHz
Phase shifter range	$>$ 360 degrees
Phase shifter resolution	$<$ 0.21 degrees/step

Table 4: Input Power Requirements

Parameter	Definition
Input voltage	115/230 VAC
Input current	2/1 A
Frequency	60/50 Hz
Voltage selection	Switch
Low voltage range	104–126 V
High voltage range	207–253 V

5 Warranty and Support

5.1 Warranty

Dimtel Inc. warranties this product for a period of one year from the date of shipment against defective workmanship or materials. This warranty excludes any defects, failures or damage caused by improper use or inadequate maintenance, installation or repair performed by Customer or a third party not authorized by Dimtel, Inc. Warrantied goods will be either repaired or replaced at the discretion of Dimtel, Inc. The above warranties are exclusive and no other warranty, whether written or oral, is expressed or implied.

5.2 Support

Dimtel Inc. will provide technical support for the product free of charge for a period of one year from the date of shipment. Such support is defined to include:

- Gain partitioning;
- System interconnection issues;
- iGp interface support.

Free of charge technical support specifically excludes:

- Commissioning with beam;
- Feedback algorithm development and testing;
- Beam dynamics characterization;
- Operational support related to dynamic system operation.

6 Glossary

Glossary

beam position monitor (BPM)

An RF structure that couples to the beam in the accelerator. The output signal of such a structure allows measurement of the transverse or the longitudinal beam position. 3, 5, 7

continuous wave (CW)

A signal of constant amplitude and frequency. 5, 7, 8

digital-to-analog converter (DAC)

A hardware device to convert a sequence of digital codes to corresponding analog voltages or currents. 5

general-purpose input/output (GPIO)

A 32-bit wide digital input/output port of the iGp. 3, 7

integrated gigasample processor (iGp)

A baseband bunch-by-bunch signal processing channel designed for longitudinal and transverse feedback applications in storage rings as well as for bunch-by-bunch diagnostics. 3, 5–9, 12, 13

MATLAB

A numerical computing environment and a programming language 8

radio frequency (RF)

In the accelerator context, a constant frequency constant amplitude signal derived from or phase locked to the storage ring master oscillator. 7, 10