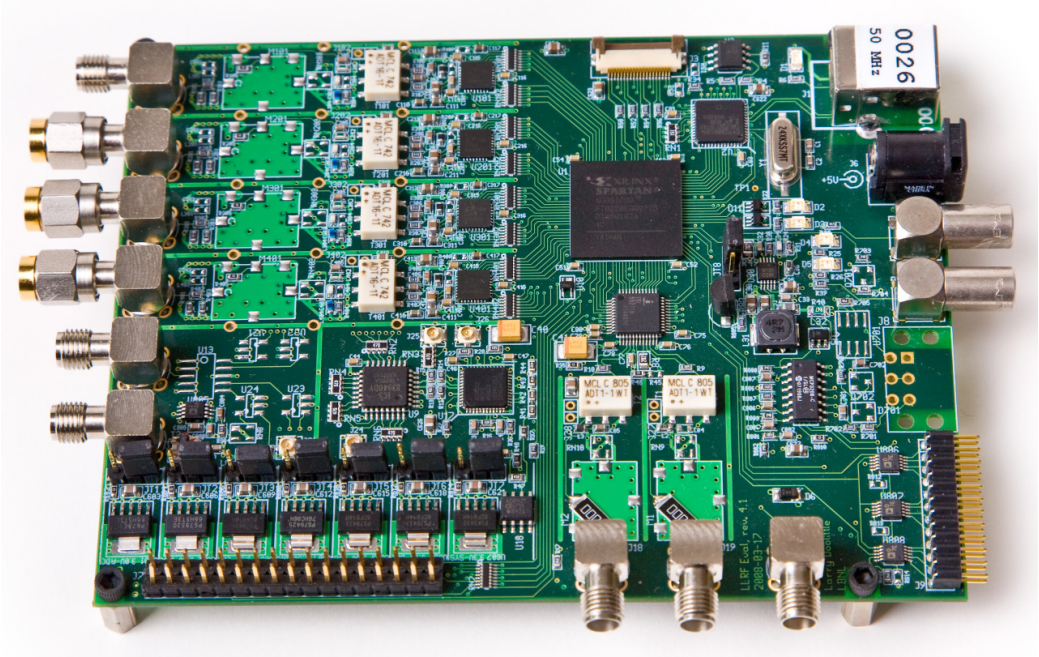

# LLRF4 Evaluation Board

USPAS Lab Reference

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1.1

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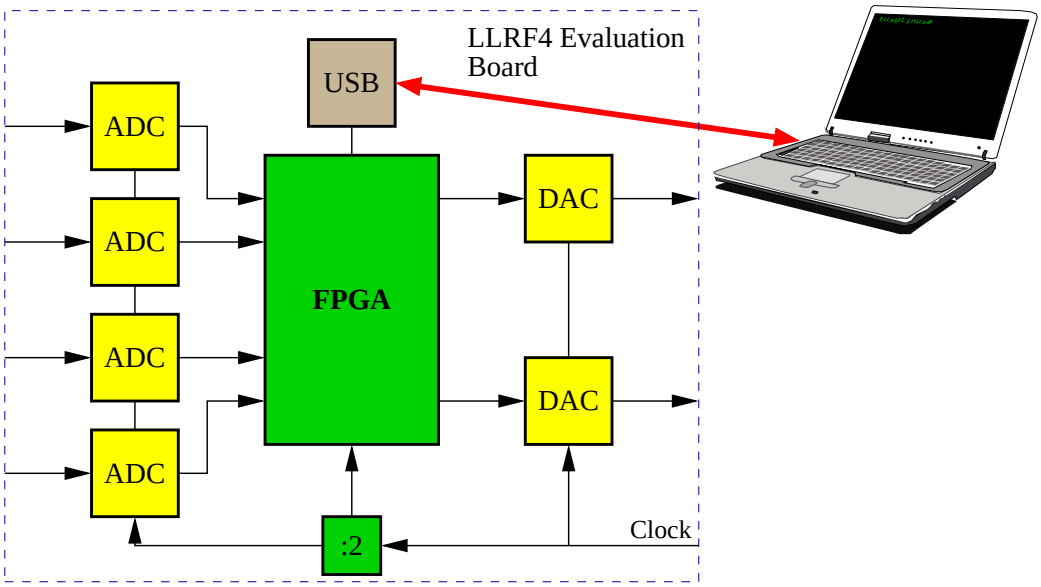


Figure 1: LLRF4 block diagram.

# 1 Introduction

Laboratory exercises for this class will extensively use an evaluation board, designed by Larry Doolittle of Lawrence Berkeley Laboratory. The board, called LLRF4, has low-level RF (LLRF) processing as its the main design application. However the structure of the board is general enough to invite other accelerator applications and to serve as a fairly universal learning platform.

A block diagram of the board is shown in Fig. 1. The board is equipped with four input analog-to-digital converter (ADC) channels and two digital-to-analog converter (DAC) outputs. Both ADCs and DACs are connected to a field programmable gate array (FPGA), which performs real-time signal processing, data acquisition, and signal synthesis. A universal serial bus (USB) port provides the board with a control and diagnostic interface.

For the USPAS class the board is configured as a signal processing demonstration module with the following features:

1. Four ADC data acquisition and display.
2. Two DAC signal generators.

3. Real-time second-order digital filter driven by ADC0.

In this short reference I will go over the above features in more detail, show the connector locations, describe the computer interface and basic operational steps.

## 1.1 Getting Started

**WARNING: LLRF4 evaluation boards are not protected in any way. Care must be taken not to bring the energized board in contact with conductive materials. Such contact can cause permanent damage to the board.**

**Before connecting the power supply, make sure there are no cables, wires, metal modules, etc. in contact with the board. Make interconnects in such a way as to minimize the possibility of hardware shifting while powered.**

**WARNING: Integrated circuits on LLRF4 board can get hot during operation. Do not touch components on the board!**

In order to get your system up and running, you should log in on the provided control laptop. Username is `llrf` and the password is `uspas`. On the desktop you will see an icon, labeled *LLRF*. Don't click on it right away — go through the checklist below first:

- Connect USB cable to the LLRF4 board and the control laptop;
- Make sure there is no metal in contact with the board - see the warning above;
- Connect the sampling clock (see Fig. 2 for connector locations);
- Connect power adapter to LLRF4. LEDs D2 and D3 should light up;
- Double-click on the *LLRF* icon. User interface panel should open in a few (5–10) seconds.

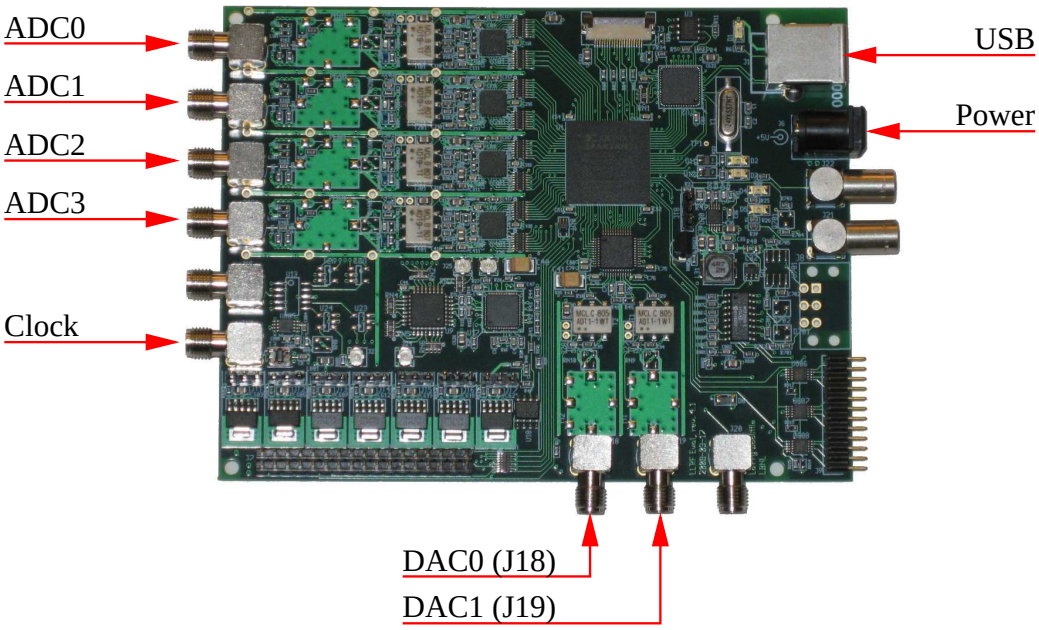


Figure 2: Connector locations.

# 2 Hardware

## 2.1 Connector locations

Locations of connectors we will be using during this class are shown in Figure 2. Additional connectors on board (not referenced on the photo) include trigger inputs and outputs, low-speed digital and analog I/O, interlocks, and other service functions.

## 2.2 Input channels

Four input channels use LTC2255 ADC s from Linear Technologies. These 14-bit converters are capable of running at 125 Mega-samples per second (MSPS). Analog inputs include bandpass filters with 48 MHz center frequency and 12 MHz 3 dB bandwidth. Full-scale input level is +9 dBm.

## 2.3 Output channels

High-speed analog outputs LLRF4 evaluation board are provided by ISL5927 dual-channel 14-bit 260 MSPS DAC from Intersil. Outputs are transformer coupled. One output channel (DAC0, connector J18) is low-pass filtered, the other channel is unfiltered. Full-scale output level of the DACs is -3.3 dBm at low frequencies. As the frequency rises the level drops due to filtering and zero-order hold (ZOH).

## 2.4 Clocking

LLRF4 board can accept input clocks up to 1.6 GHz and has provisions for dividing down the clock. Since high-speed DACs are capable of twice the update rate of the ADCs, the DAC clock is normally twice the frequency of the ADC and the FPGA one. In this class we will use 250 MHz clock signal, so that internal division ratio is two for ADC and FPGA clocks and one for the DAC.

## 2.5 FPGA

Figure 3 shows the block diagram of the functionality implemented in the FPGA. Data from each ADC is routed to at least two destinations: dual-port data acquisition memory and the root mean square (RMS) monitor. ADC0 also serves as the signal source for a second-order infinite impulse response (IIR) filter block.

RMS monitor performs ADC data squaring and long-term averaging, applying a rectangular window of adjustable length. Typical window length is 100–500 ms, matched to 10 Hz RMS register polling rate.

Two DAC outputs are driven using dual data rate (DDR) capabilities to output two samples each ADC clock period, since DAC clock is twice as fast. For each DAC one of the four signal sources can be selected:

**IIR**
: Output of the digital filter. This output is updated at the ADC clock rate, so the effective update rate of the DAC is 125 MSPS.

**DDS**
: Output of a direct digital synthesis (DDS) signal generator. The gen-

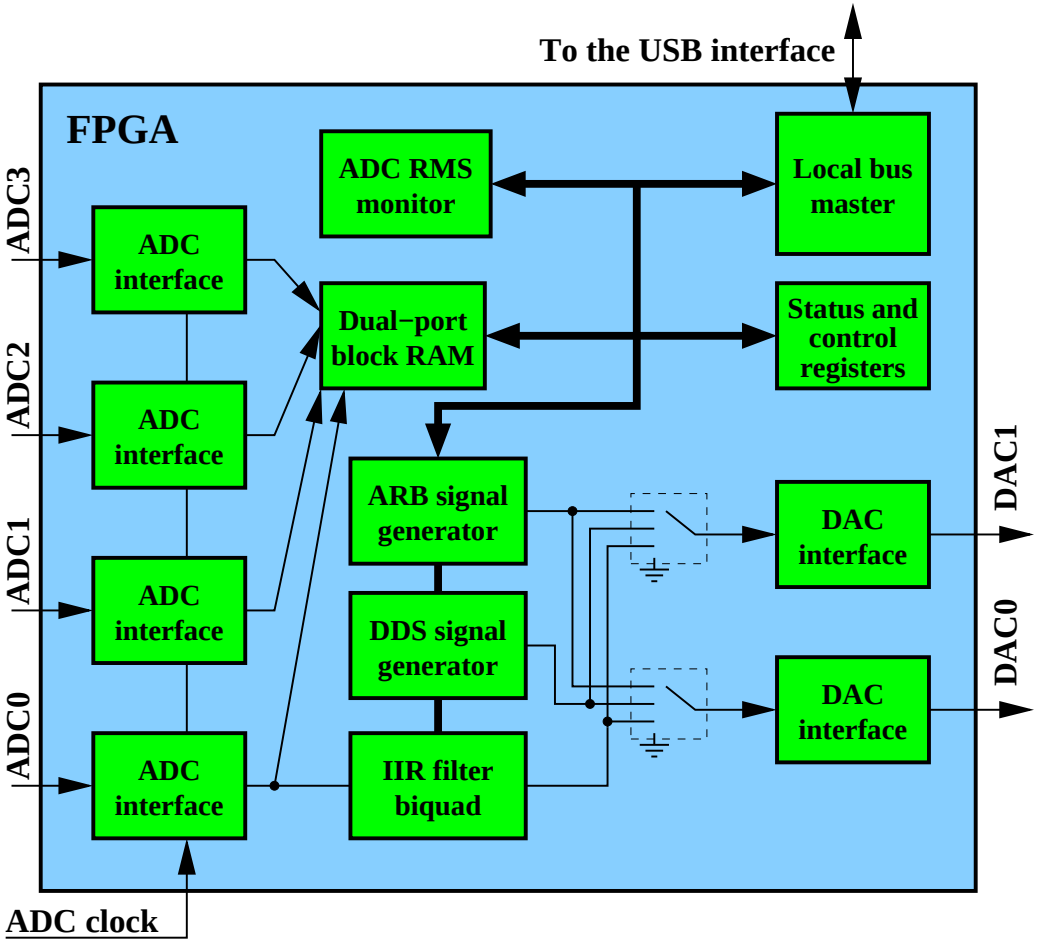


Figure 3: FPGA block diagram.

erator produces sine and square wave outputs at the full DAC rate (250 MSPS).

**ARB**
Output of an arbitrary waveform generator. This generator also runs at 250 MSPS and is based on 2048-sample waveform memory.

**OFF**
This option set the DAC data stream to zero.

# 3 Acquisition

In USPAS configuration, ADC data acquisition is done in two independent paths: raw waveform capture and RMS measurement. Let's consider each of these in turn.

## 3.1 Waveform capture

This data acquisition feature captures fixed waveform snapshots simultaneously for all four ADCs. Each ADC is allocated a 4096 sample buffer (32.8 $\mu$s). experimental physics and industrial control system (EPICS) software triggers data acquisition and then reads out the waveform buffers. The data is presented to the user in time domain as waveform displays and in frequency domain as Fourier transform magnitude. Acquisitions and readouts are performed at 10 Hz rate.

## 3.2 RMS measurements

A separate data acquisition path performs RMS measurements. These measurements are generated by a squaring block, followed by an adjustable cascaded integrator comb (CIC) decimation filter. Filter averaging time can be adjusted from control panels. Since RMS registers are polled at 10 Hz, averaging time should be at least 100 ms. Longer averaging times will further reduce the aliasing.

# 4 Synthesis

FPGA gateware include two independent waveform synthesizers: DDS and memory based ones (DDS and ARB on the block diagram and control panels). Each signal generator has strengths and weaknesses which will be explored in detail during the DAC laboratory on Tuesday.

## 4.1 ARB signal generator

Arbitrary waveform generator in LLRF4 is based on 2048 sample waveform memory. The memory is continuously played back at the DAC sampling rate of 250 MSPS. This architecture allows one to generate a wide variety of

waveforms, but imposes significant restrictions. The most severe one is that the generated frequencies have to be periodic over 2048 samples. For sine waves that requirement leads to quantization of allowable frequencies with the step of $f_{\mathrm{DAC}}/2048 = 122$ kHz.

## 4.2 DDS signal generator

DDS generator is limited to producing sine or square wave shapes. At the same time, frequency resolution is excellent. In the range of DC to $f_{\mathrm{DAC}}/2$ the maximum error between setpoint and generated frequency is 0.23 Hz. For most settings the error is sub-mHz.

# 5 Real-time processing

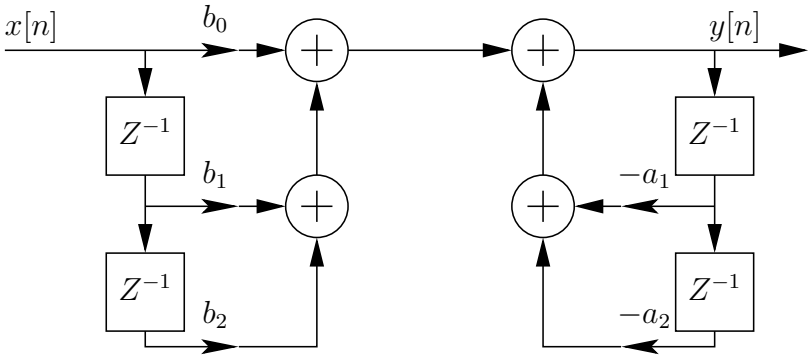


Figure 4: IIR biquad implementation.

Real-time signal processing in LLRF4 is implemented as a single IIR filter in a general second-order section form (biquad). The filter is implemented in Direct Form I, as shown in Figure 4. The section implements a second-order polynomial transfer function:

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} = \frac{b_0 z^2 + b_1 z + b_2}{z^2 + a_1 z + a_2} \tag{1}$$

This implementation form was chosen so that saturation could be effectively controlled in the channel by adjusting the gains in the numerator (finite impulse response (FIR)) section. Coefficients $b_0$, $b_1$, $b_2$, $a_2$ can range from -1

to 1. Coefficient $a_1$ magnitude is limited to 2. These choices allow one to implement any stable IIR response function.

# 6 EPICS

LLRF4 board is controlled through EPICS interface running under extensible display manager (EDM). In this section you will find full descriptions of all interface panels and all control and readout elements.

## 6.1 Main panel

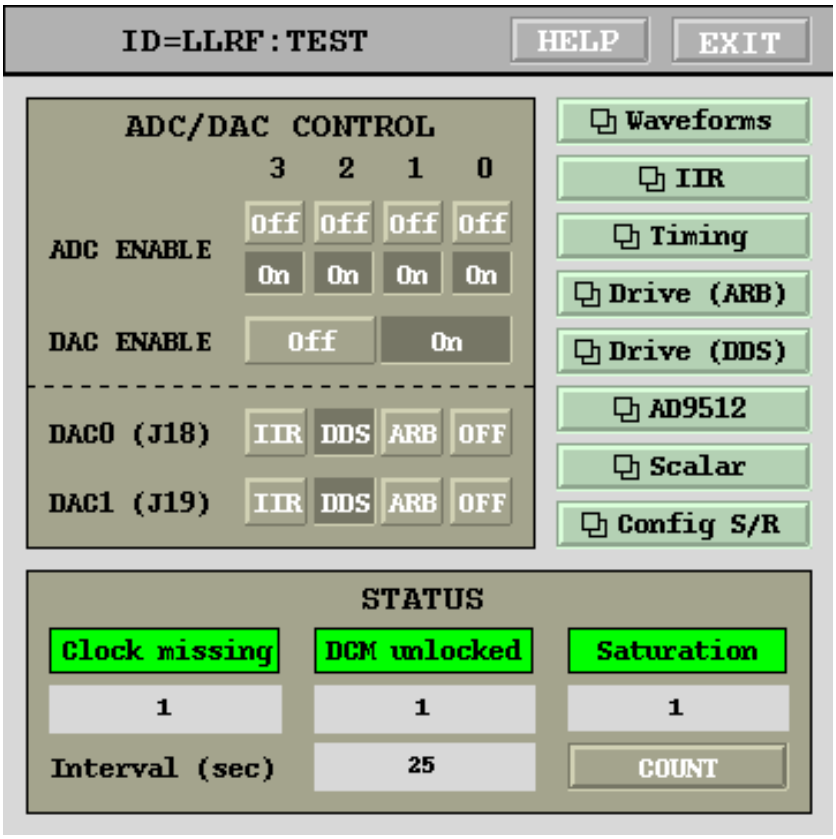


Figure 5: Top control panel.

Top control panel, shown in Figure 5, is the one you get when you start the board. It combines status/error displays and counters, controls of ADCs and DACs and is a gateway to all other system panels. `EXIT` button causes EDM to exit and closes all open EPICS panels.

**ADC ENABLE**
This control turns on or off the power to individual ADCs. At full 125 MSPS rate the ADCs dissipate quite a bit of power, so if you are not using a channel — turn it off and the board will run a bit cooler!

**DAC ENABLE**
This controls power state of the output dual-channel high-speed DAC.

**DAC0 (J18)**
Four-way data source selector for DAC channel 0.

**DAC1 (J19)**
Four-way data source selector for DAC channel 1.

**Clock missing**
This error indicator turns red if the input clock is not detected. This could be an indication of disconnected clock, low signal level, or incorrect frequency. All status indicators are polled at 1 Hz.

**DCM unlocked**
digital clock manager (DCM) within the FPGA is used to optimally align the signal processing clock with the ADC data. If the clock is intermittent, DCM can lose lock. `DCM RESET` button on the timing panel can be used to force resynchronization.

**Saturation**
This indicator turns red if the IIR filter output is hitting full scale. Saturator circuit clips the output at positive or negative full scale and reports the error. Reduce input level or gain if saturation is happening.

**COUNT**
This button reset error and interval counters.

**Waveforms**
Opens the waveform window.

**IIR**
Opens the IIR control panel.

**Timing**
Opens the timing control panel.

**Drive (ARB)**
Opens the arbitrary waveform generator panel.

**Drive (DDS)**
Opens the DDS control panel.

**AD9512**
Opens the control panel for Analog Devices AD9512 clock distribution chip.

**Scalar**
Opens the RMS panel.

**Config S/R**
Opens the dialog for saving or restoring system configuration.

## 6.2 Waveforms panel

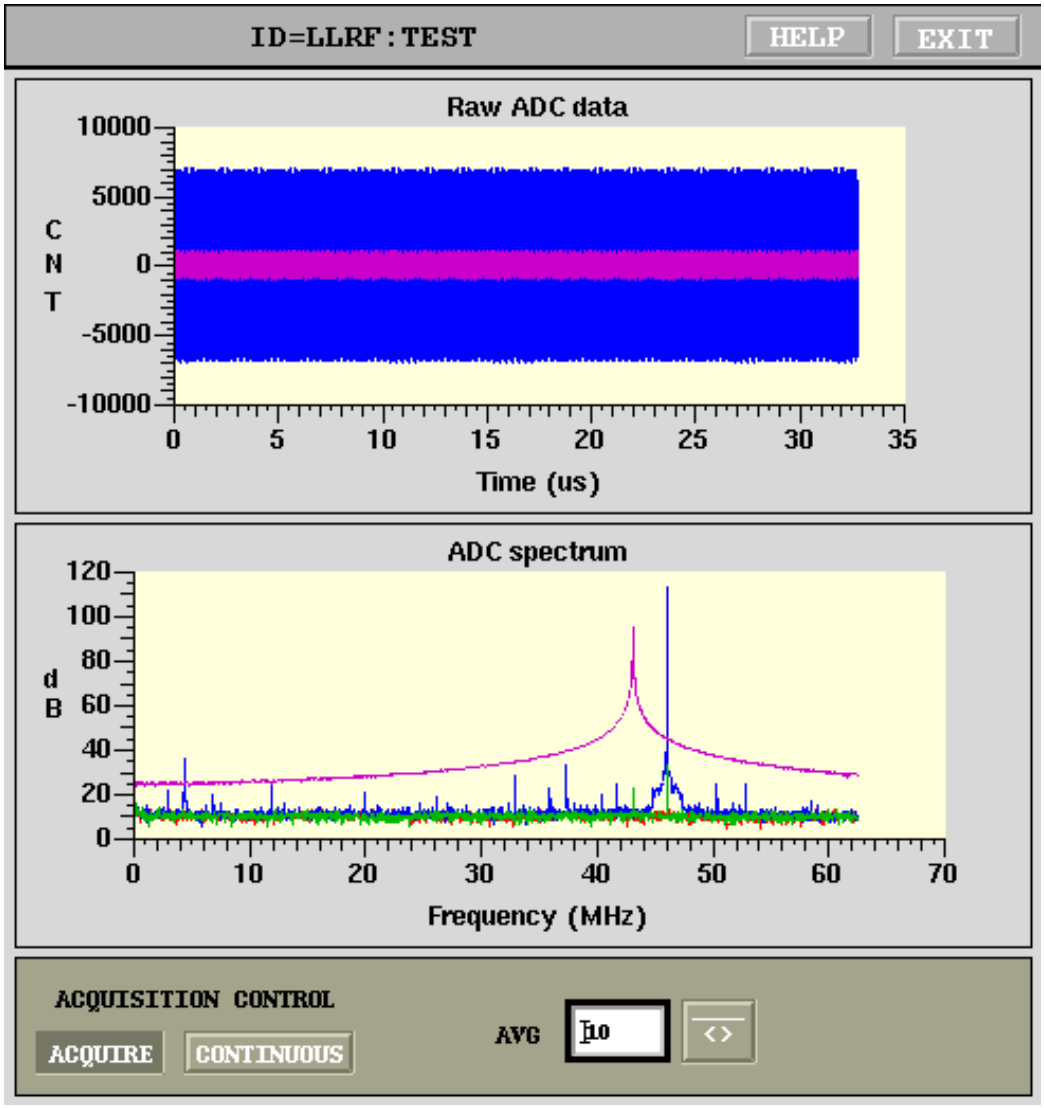


Figure 6: Waveforms panel.

This panel controls the data acquisition and post-processing. Acquired waveforms and spectra are displayed in this window. The top plot shows the raw ADC data versus time. All four channels are plotted. If the ADC for

the particular channel is turned off, it's data stream is simply zeroes.

The bottom plot shows the Fourier transforms of the time-domain signals. The horizontal scale is frequency in MHz and the vertical scale is magnitude in dB.

Acquisition control has two buttons: `ACQUIRE/OFF` and `CONTINUOUS/SINGLE`. In continuous mode, if `ACQUIRE/OFF` is set to `ACQUIRE`, the board performs data acquisition and readout at 10 Hz. Acquisition can be stopped by setting `ACQUIRE/OFF` to `OFF`. In `SINGLE` mode, acquisition stops automatically after one trigger/readout cycle and `ACQUIRE` button changes state to `OFF`.

`AVG` control is used to adjust the averaging time constant on the spectral display. The setpoint value is the time constant is acquisitions. Value of 10 corresponds to a time constant of 1 second at 10 Hz update rate.

## 6.3 IIR panel

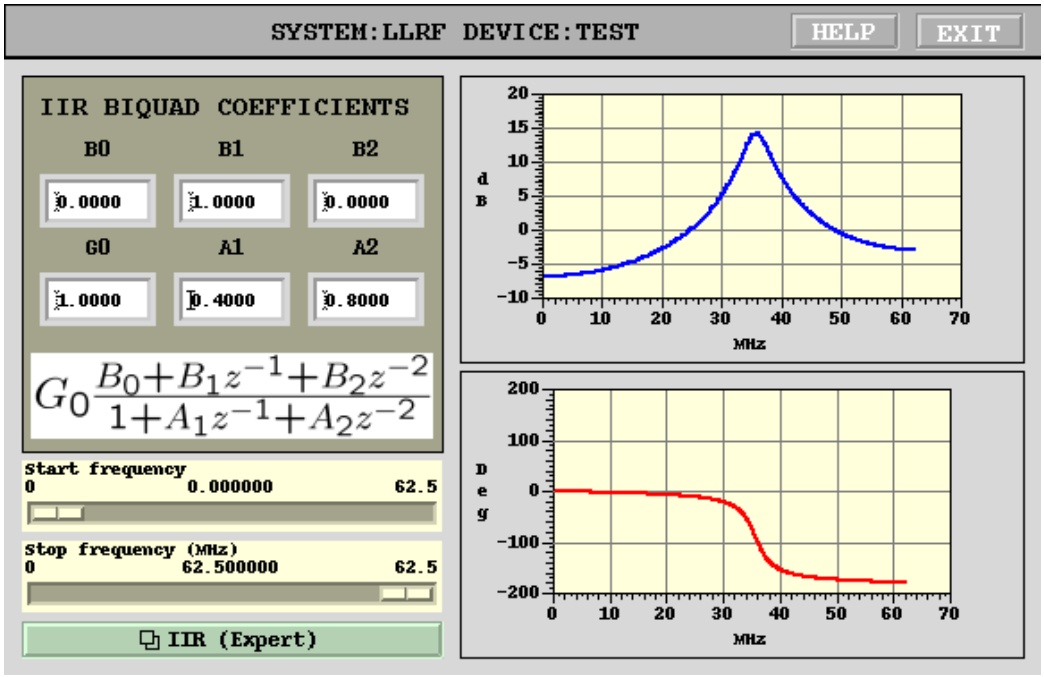


Figure 7: IIR panel.

The IIR panel has entry fields for five coefficients of an IIR filter, as described in Section 5. Additional setting of gain, `G0` is used to scale the numerator coefficients together, providing a convenient way to adjust overall gain. Magnitude and phase response of the filter is computed and plotted every time the coefficients are changed. Each plot samples the frequency range at 512 points. For very narrow filters that might be insufficient to resolve the peaks or notches properly. Start and stop frequency sliders allow to zoom in on a section of a frequency range. Zooming in from a full span of 62.5 MHz to a span of 1 MHz will change the frequency sampling step from 122 to 2 kHz.

## 6.4 Timing

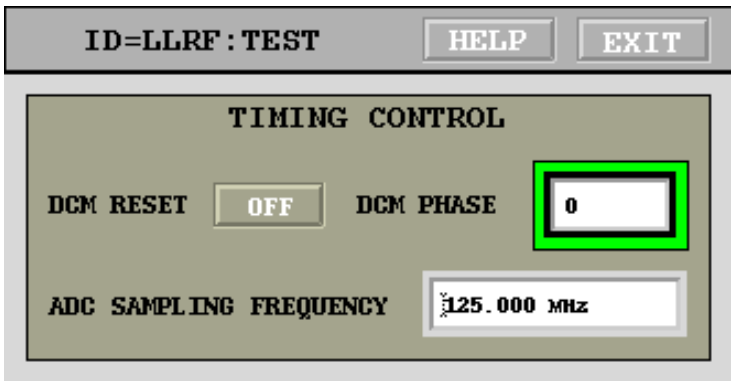


Figure 8: Timing panel.

On this panel, shown in Figure 8 one can adjust the FPGA clock phase, specify appropriate sampling frequency, and perform DCM reset. During this class you should not need to use this panel.

## 6.5 Arbitrary waveform generator

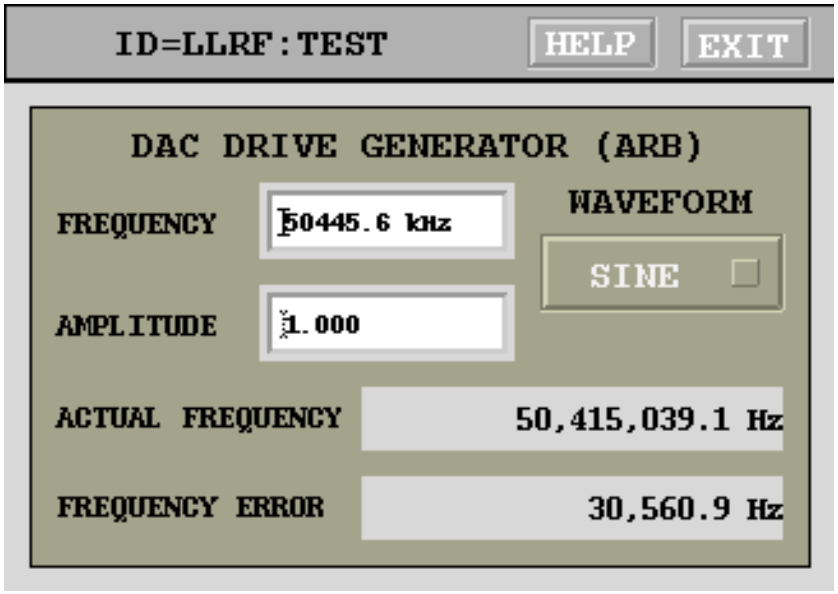


Figure 9: Arbitrary waveform generator panel.

Using this panel one can adjust the setting of the memory-based arbitrary waveform generator.

**FREQUENCY**
: Output signal frequency setting in kHz, used in sine, square, and sawtooth modes.

**AMPLITUDE**
: Output amplitude, one corresponds to DAC full scale.

**WAVEFORM**
: Selects one of four possible waveform types: `SINE`, `SQUARE`, `SAWTOOTH`, and `ARB`. In the first three modes, the EPICS controller generates the waveform based on the specified amplitude and frequency. In the `ARB` mode the sample values are taken from 2048-element waveform record LLRF:TEST:DRIVE:ARB.

**ACTUAL FREQUENCY**
: This readback displays the actual output frequency. Frequency is constrained by the waveform memory length and periodicity requirement.

It is further constrained by the even period requirement for the square and sawtooth waveforms (highest frequency square wave is two samples, next down is four samples, and so on).

**FREQUENCY ERROR**

Error between setpoint and generated frequencies.

## 6.6 DDS signal generator

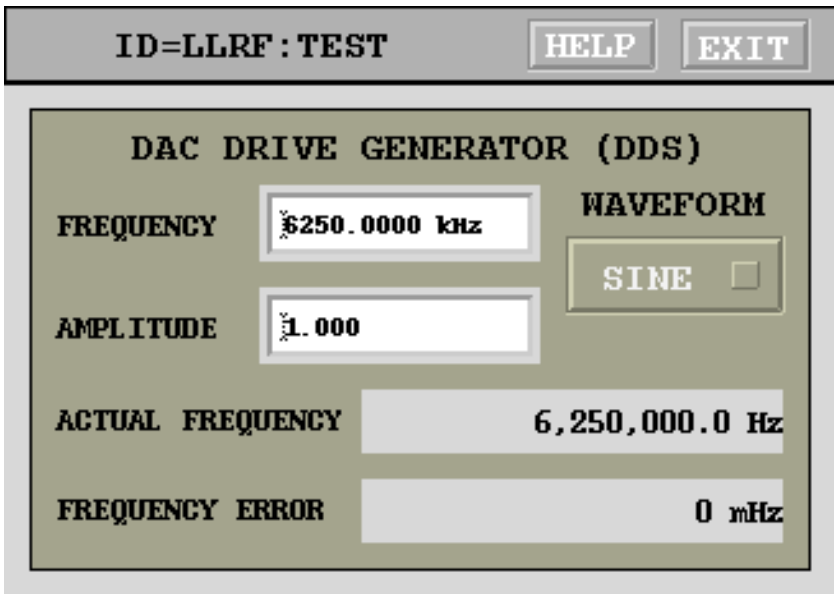


Figure 10: DDS signal generator panel.

DDS signal generator control panel, shown in Fig. 10 is quite similar to the arbitrary waveform panel described above.

**FREQUENCY**
Output signal frequency setting in kHz.

**AMPLITUDE**
Output amplitude, one corresponds to DAC full scale.

**WAVEFORM**
Selects one of two possible waveform types: `SINE` or `SQUARE`.

**ACTUAL FREQUENCY**
This readback displays the actual output frequency.

**FREQUENCY ERROR**
Error between setpoint and generated frequencies (note the units).

## 6.7 AD9512 controls

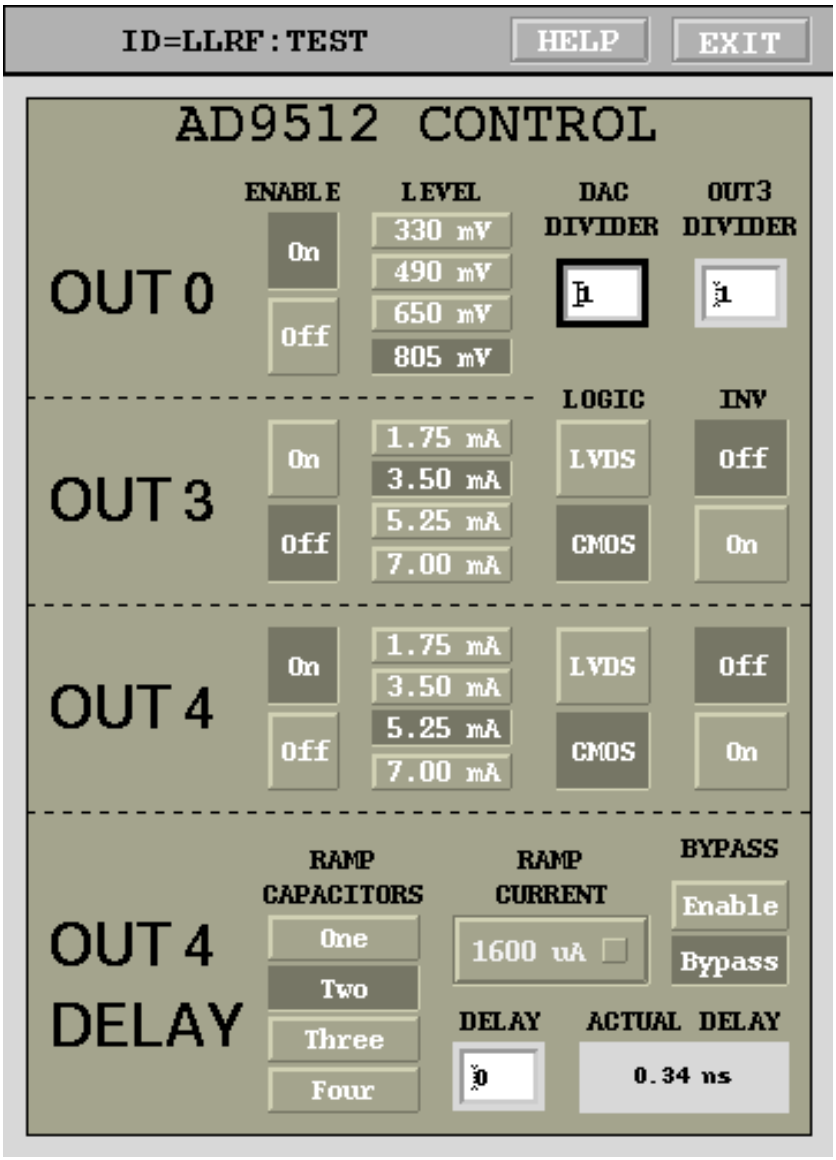


Figure 11: Clock distribution chip controls.

This panel provides controls for configuring the Analog Devices AD9512 clock distribution chip on LLRF4. Output 0 drives the ADCs and the FPGA. Output 4 clocks the DAC. `DAC DIVIDER` setting controls the input clock

divide ratio. For our labs we will use the ratio of 1 with 250 MHz input clock, giving us 250 MHz DAC and 125 MHz ADC clocks. Setting this to 2, for example, would produce 125 and 62.5 MHz DAC and ADC clocks respectively.

## 6.8 RMS monitoring

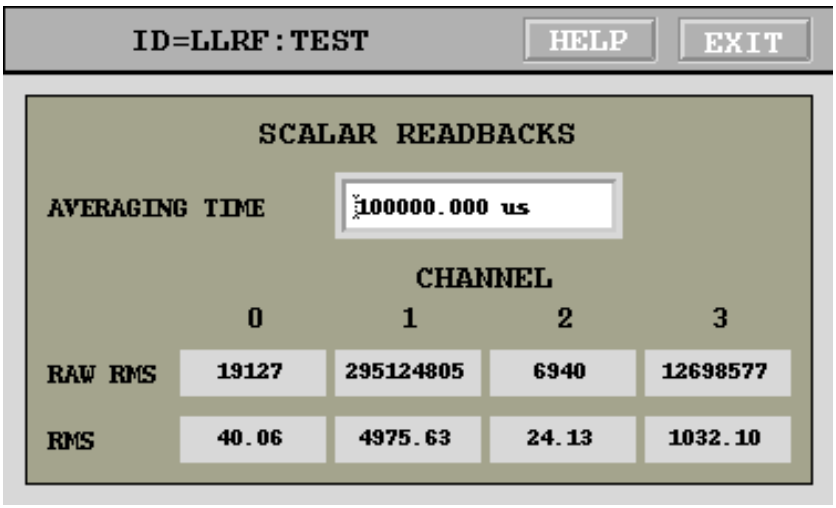


Figure 12: RMS monitoring panel.

This panel presents the RMS measurements, updated at 10 Hz. The measurement itself is performed by the FPGA in real-time and is then decimated for the readout.

**AVERAGING TIME**
: Time in microseconds to average the readout. To minimize aliasing this setting should be above 100 ms.

**RAW RMS**
: Values, read out from the hardware register. These will change scale as a function of averaging time.

**RMS**
: True RMS of the ADC signals, in ADC counts.

## 6.9 Save/restore panel.

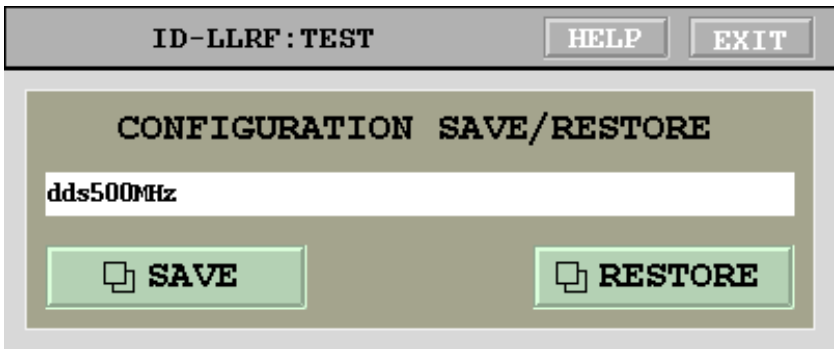


Figure 13: Save/restore panel

This panel allows the user to save and restore named configurations. Clock on the light beige entry field to bring up file selection dialog. Once the file name is set, one can save or restore the configuration by clicking the appropriate button.

# 7 Glossary

## Glossary

**analog-to-digital converter (ADC)**

An electronic circuit that converts continuous analog signals to discrete digital numbers. 2, 4–7, 10, 11, 13, 20, 22, 25

**cascaded integrator comb (CIC)**

An efficient multiplier-less implementation of long impulse response low-pass filter. 7

**digital-to-analog converter (DAC)**

A hardware device to convert a sequence of digital codes to corresponding analog voltages or currents. 2, 4–7, 10, 11, 17, 19, 20, 25

**digital clock manager (DCM)**

A delay-locked loop (DLL) based clock management circuit integrated in the Xilinx® FPGA. The circuit allows fine phase adjustment of the output clock relative to the input. 11, 16

**dual data rate (DDR)**

A method of transferring two bits of information every clock cycle on a single wire by changing the value on both rising and falling edges of the clock. 5

**direct digital synthesis (DDS)**

A technique for generating arbitrary frequencies and waveforms from a fixed-frequency clock source. 5, 7, 8, 12, 19

**delay-locked loop (DLL)**

A device for managing clock skew in digital circuits. 24

**extensible display manager (EDM)**

A tool that manages a collection of active displays with the ability to create and edit display content as well as the ability to execute the same content resulting in the dynamic presentation of live data. 10

**experimental physics and industrial control system (EPICS)**

A set of software tools and applications used to develop distributed soft real-time control systems. 7, 10, 17

**finite impulse response (FIR)**

A discrete-time filter, output of which only depends on a finite number of previous input samples. 8, 25

**field programmable gate array (FPGA)**

A semiconductor device containing programmable logic components and programmable interconnects. 2, 5, 11, 16, 20, 22

**infinite impulse response (IIR)**

A discrete-time filter, output of which depends on an infinite number of previous input samples. Unlike FIR filters, IIR structures involve internal feedback. 5, 8, 11, 15

**low-level RF (LLRF)**

A subsystem responsible for measuring cavity fields and generating drive signals for the high-power radio frequency (RF) 2

**Mega-samples per second (MSPS)**

ADC and DAC conversion rate is typically specified in units of conversions per second. 4

**radio frequency (RF)**

In the accelerator context, a constant frequency constant amplitude signal derived from or phase locked to the storage ring master oscillator. 25

**root mean square (RMS)**

A statistical measure of the magnitude of a varying quantity. 5–7, 12, 22

**universal serial bus (USB)**

A serial bus standard to interface a wide variety of devices. 2

**zero-order hold (ZOH)**

A method of converting discrete-time signals to continuous-time by holding constant sample value for one sample interval. 4